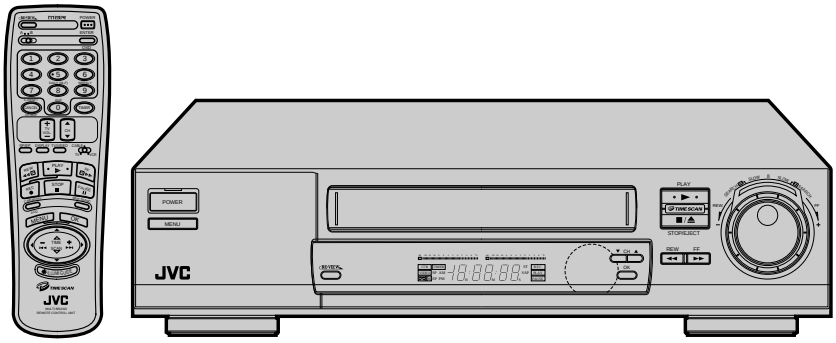
JVC

VIDEO TECHNICAL GUIDE

VIDEO CASSETTE RECORDER

HR-VP830U/E939EG/J936MS NTSC/PAL/SECAM



VCR Plus+ c3 w/Cable Channel Changer

Hi-Fi VHS

TIME SCAN

No.VTG82081
April 1997

TABLE OF CONTENTS

SECTION 1
FEATURES

1.1 FEATURE COMPARISON TABLE

		Best picture		DD Drum
	Model Name	Auto carriblation	Auto picture	
U/U(C)	HR-S9400U	Yes	Yes	Yes
	HR-S7300U	-	-	-
	HR-S5300U	-	-	-
	HR-VP830U/U(C)	Yes	Yes	Yes
	HR-VP639U/U(C)	No	Yes	No
	HR-VP638U/U(C)	No	Yes	No
	HR-VP82U	No	Yes	No
	HR-VP636U/U(C)	Yes	Yes	No
	HR-VP634U	Yes	Yes	No
	SR-3360U	Yes	Yes	No
	HR-633U/U(C)	Yes	Yes	No
	HR-630U/U(C)	No	Yes	No
	HR-A62U	No	No	No
	HR-A52U/U(C)	No	No	No
	HR-VP436U	Yes	Yes	No
	HR-VP434U	Yes	Yes	No
	HR-J433U/U(C)	Yes	Yes	No
	HR-J430U	Yes	Yes	No
	HR-A42U	No	No	No
	HR-A32U	No	No	No
	HR-A22U/U(C)	No	No	No
UM	HR-J6003UM	Yes	Yes	No
	HR-J4003UM	Yes	Yes	No
M	HR-J836M	Yes	Yes	No
	HR-J636M	Yes	Yes	No
	HR-J633M	Yes	Yes	No
	HR-J536M	Yes	Yes	No
	HR-J436M	Yes	Yes	No
	HR-J433M	Yes	Yes	No
EG	HR-E939EG	Yes	Yes	Yes
	HR-E439EG	Yes	Yes	No
	HR-E239EG	Yes	Yes	No
ES	HR-A230ES	No	No	No
E/EH	HR-E939EH	Yes	Yes	Yes
	HR-J638E	Yes	Yes	No
	HR-J638EH	Yes	Yes	No
	HR-A637E	No	No	No
	HR-A637EH	No	No	No
	HR-J438E	Yes	Yes	No
	HR-A437E	No	No	No
	HR-A433E	No	No	No
	HR-A430E	No	No	No
	HR-J238E	Yes	Yes	No
	HR-A237E	No	No	No
	HR-A233E	No	No	No
	HR-A230E	No	No	No

Table 1-1-1 Feature comparison table (1/2)

• FEATURE COMPARISON TABLE

	Model Name	Best picture		DD Drum
		Auto carriblation	Auto picture	
EK	HR-J935EK	Yes	Yes	Yes
	HR-J635EK	Yes	Yes	No
	HR-A631EK	No	No	No
	HR-A630EK	No	No	No
	HR-J435EK	Yes	Yes	No
	HR-J235EK	Yes	Yes	No
	HR-A231EK	No	No	No
	HR-A230EK	No	No	No
MS	HR-S8000MS	No	No	No
	HR-J936MS	Yes	Yes	Yes
	HR-J636MS	Yes	Yes	No
	HR-A630MS	No	No	No
	HR-A630MS(C)	No	No	No
	HR-J536MS	Yes	Yes	No
	HR-J436MS	Yes	Yes	No
	HR-A430MS	No	No	No
	HR-J236MS	Yes	Yes	No
	HR-A230MS	No	No	No
A/K	HR-P91K	No	No	No
	HR-P71K	No	No	No
	HR-P61K	No	No	No
	HR-P41A	No	No	No
	HR-P51A	No	No	No
EE	HR-P111EE	No	No	No
	HR-E639EE	Yes	Yes	No
	HR-E539EE	Yes	Yes	No
	HR-J439EE	Yes	Yes	No
	HR-J239EE	Yes	Yes	No
A	HR-J837MS	Yes	Yes	No
	HR-J737MS	Yes	Yes	No
	HR-J237MS	No	No	No
	HR-J231MS	No	No	No
EM	HR-J437MS	No	No	No
	HR-J332EM	No	No	No
	HR-J331EM	No	No	No
ED	HR-J83MS	Yes	Yes	No
	HR-J73MS	Yes	Yes	No
K	HR-J730KR	Yes	Yes	No
	HR-J430KR	Yes	Yes	No
T	HR-J631T	Yes	Yes	No
EA	HR-J635EA	Yes	Yes	No
	HR-J435EA	No	No	No
SA	HR-J231SA	No	No	No

Table 1-1-1 Feature comparison table (2/2)

SECTION 2
THE DYNAMIC DRUM (DD) SYSTEM

This section is experience for HR-VP830u as an example.
The dynamic drum (DD) system is a forward looking development that further expands the enjoyment of the VHS Format. The mechanism greatly advances the performance and functions of VHS.

2.1 DD SYSTEM FEATURES

Previous home video equipment used a fixed drum transport system for recording and playback. While generally acceptable, in modes other than normal playback (e.g., variable speed, forward and reverse search, etc.), noise appeared in the picture and applications toward high picture quality, ease of use, and other refinements were limited.
The dynamic drum system incorporates a movable video head drum while retaining the control precision of a fixed drum. During variable speed playback in the previous system, each video head traced more than one recorded track of the tape, thus rendering high precision head tracing fundamentally impossible. The result was the appearance of disturbing bar noise in the picture.

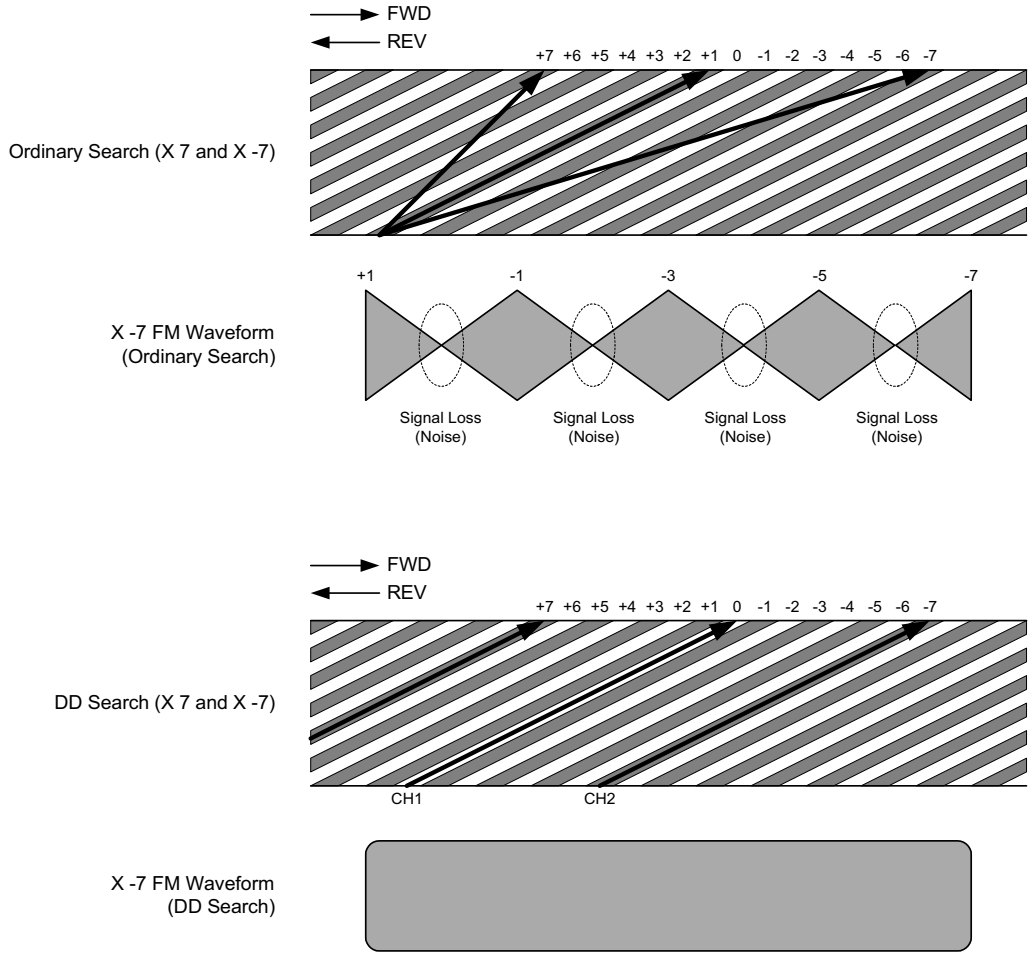


Fig. 2-1-1 Video head trace (ordinary search)

In the DD system, the entire head drum is moved dynamically to precisely align the head trace with the tape pattern and enable noise free variable speed playback.
The DD system operates during still, forward and reverse slow motion, reverse playback, 2× playback, and forward and reverse 3,5 and 7 times search (standard and 3×) modes to allow enjoying pictures free from bar noise.

Drum movement in the DD system is on the order of microns for correcting bar noise. The technological achievement results from JVC's continuous efforts in pursuit of high quality video.

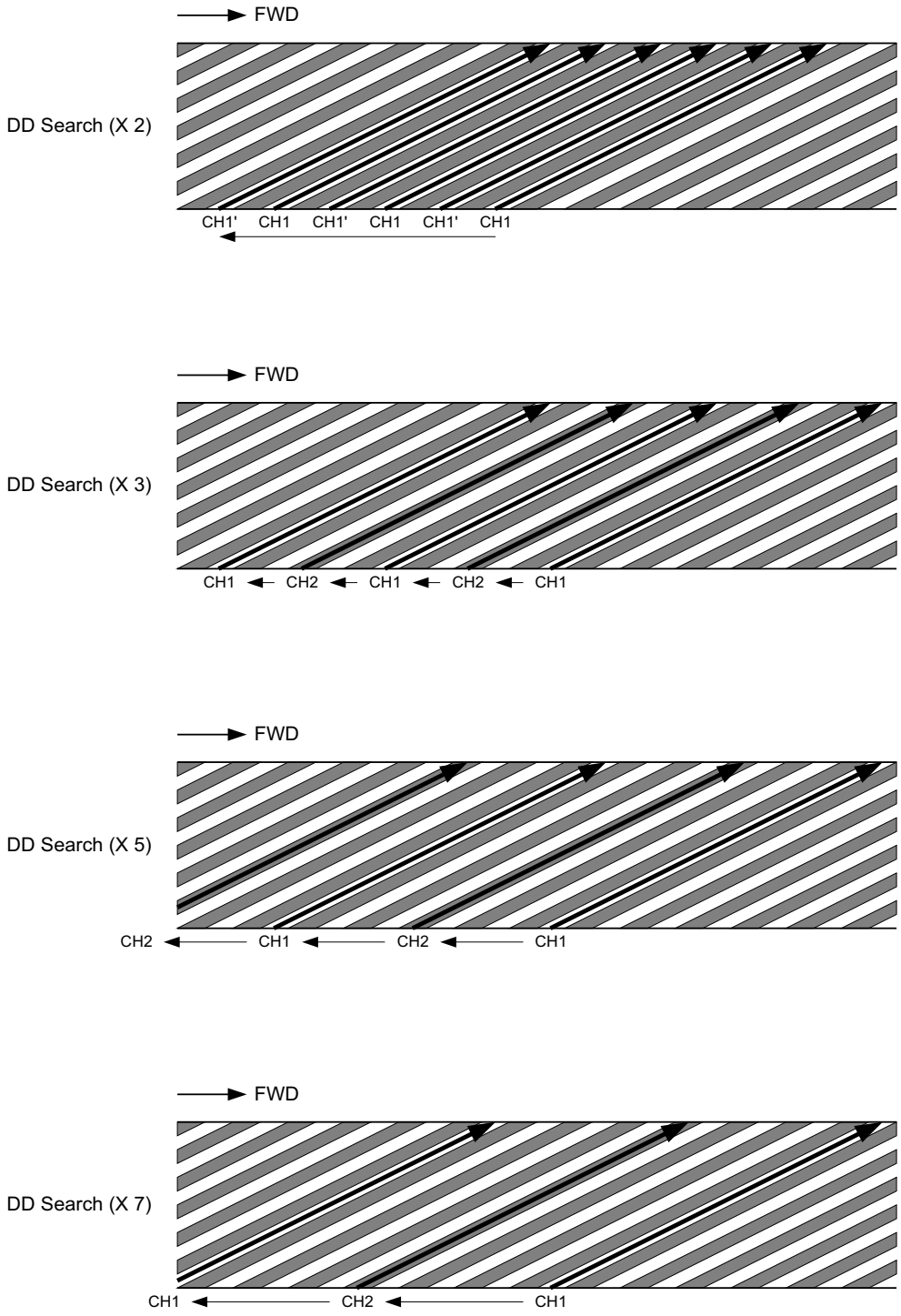


Fig. 2-1-2 Video head trace (DD search)

2.2 DD MECHANICAL SYSTEM

The previous head drum assembly comprised a fixed lower drum containing the tape lead and a rotating upper drum mounted atop this in order to maintain mounting precision. The DD system maintains mounting precision while enabling a movable drum by providing the tape lead on an independent base and setting the upper drum atop this. During operation, the lead and lower drum, and unitized upper drum provide precision control.

The drum is supported by 8 pivots, 4 each on the base and lead, and pressed by springs to ensure proper contact. The lead is pressed against the drum by 4 pivots, while the overall structure rests on the base at 4 pivots. These 8 pivots determine the accurate position, while the strong springs provide firm support. The pivots are pressed and secured during normal recording and playback.

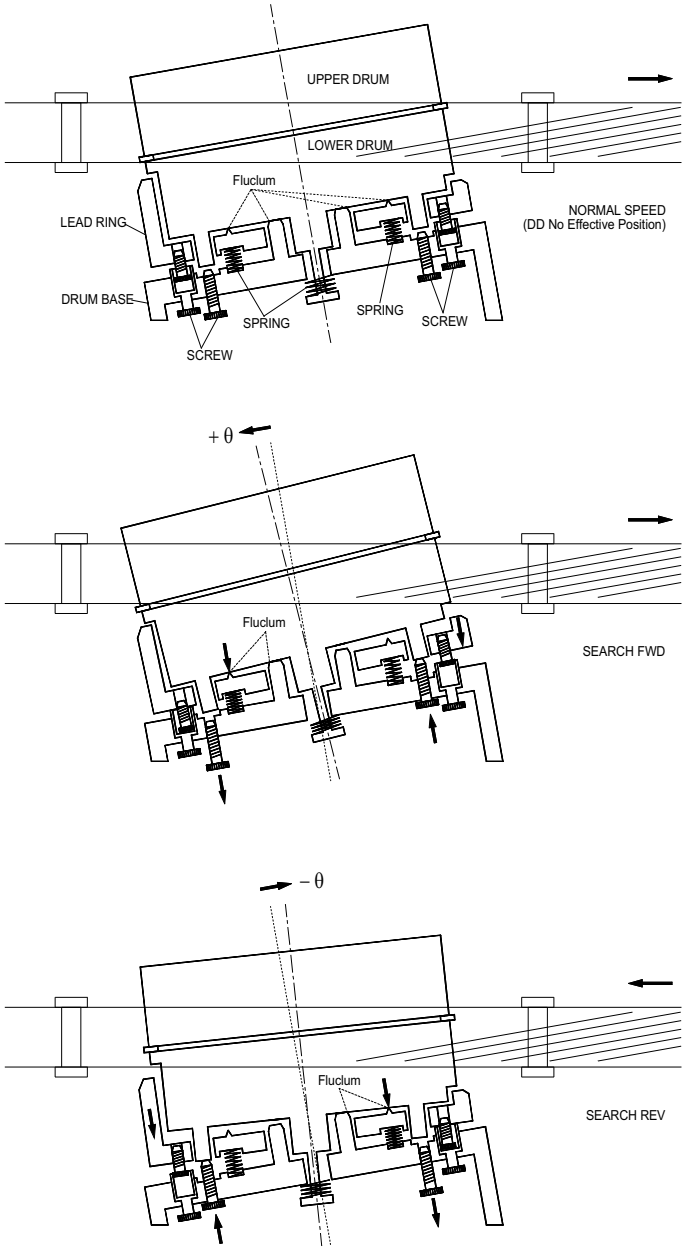


Fig. 2-2-1 Dynamic drum action

Strong torque is generated by the motor provided under the diecast base and gear assembly. The pin height is changed, and by changing the lead and drum inclination, the drum left to right angle is changed as viewed from the mechanism front. This operation is illustrated in Fig. 2-2-1.

The lead and drum inclination can be noted in the comparison of Fig. 2-2-1. The lead and drum move separately and the inclination changes. By controlling each independently, smooth operation is achieved without tape path distortion. Although the drum rides on two pivots when inclined, springs press against the drum to prevent instability. Even when inclined, firm support is provided by the pivots and adjustment pin.

The actual movement amount is in micron units. The threaded coupling pin is driven by the motor and rotates for microscopic up and down control.

In terms of the mechanism, the technology for controlling the drum inclination in micron units is not unduly complex. The overall mechanism itself is not redesigned, but only the vicinity of the drum. Since the previous mechanism can be used, precision operation is achieved without extensive manufacturing cost.

As indicated in Fig. 2-2-2, the lower drum assembly comprises a motor and gears for inclining the drum, a reset sensor for detecting the initialized position, and a pulse counter for detecting the amount of inclination. (The entire assembly is replaced at one time.)

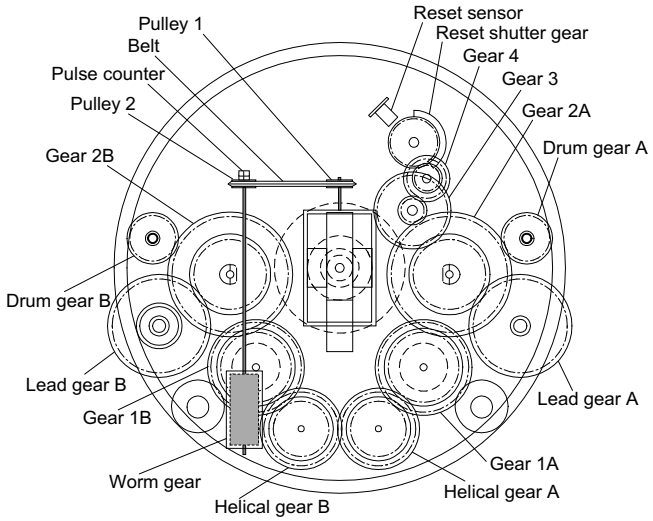


Fig. 2-2-2 Bottom view of lower drum assembly

Fig. 2-2-3 shows the exploded view of DD system. and Fig. 2-2-4 shows lower drum assembly of DD system.

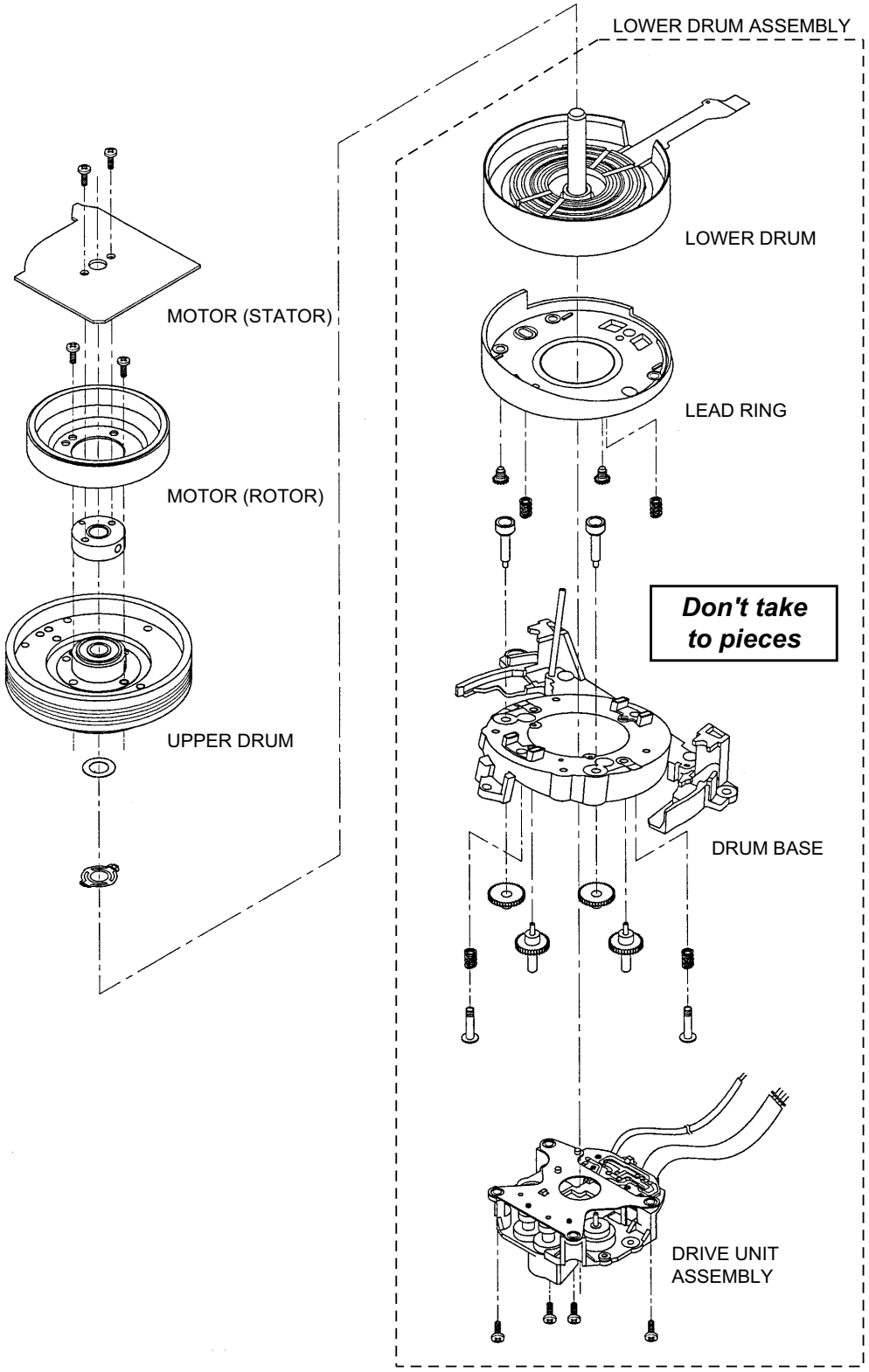


Fig. 2-2-3 Exploded view (dynamic drum assembly)

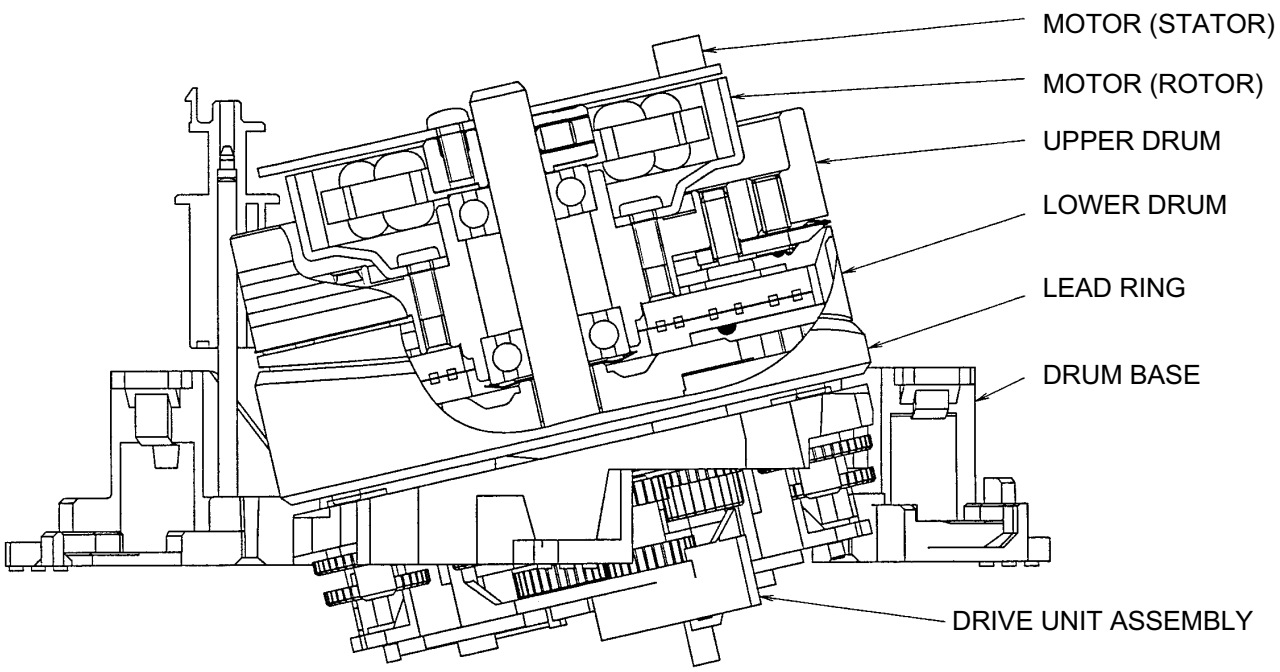


Fig. 2-2-4 Dynamic drum (lower drum) assembly

2.3 SYSTEM CONTROL

Fig. 2-3-1 shows the system control block diagram.

IC801 (sub-CPU) basically controls the DD.
IC401 controls the capstan and drum servos.
IC701 (main CPU) controls the overall set systems.

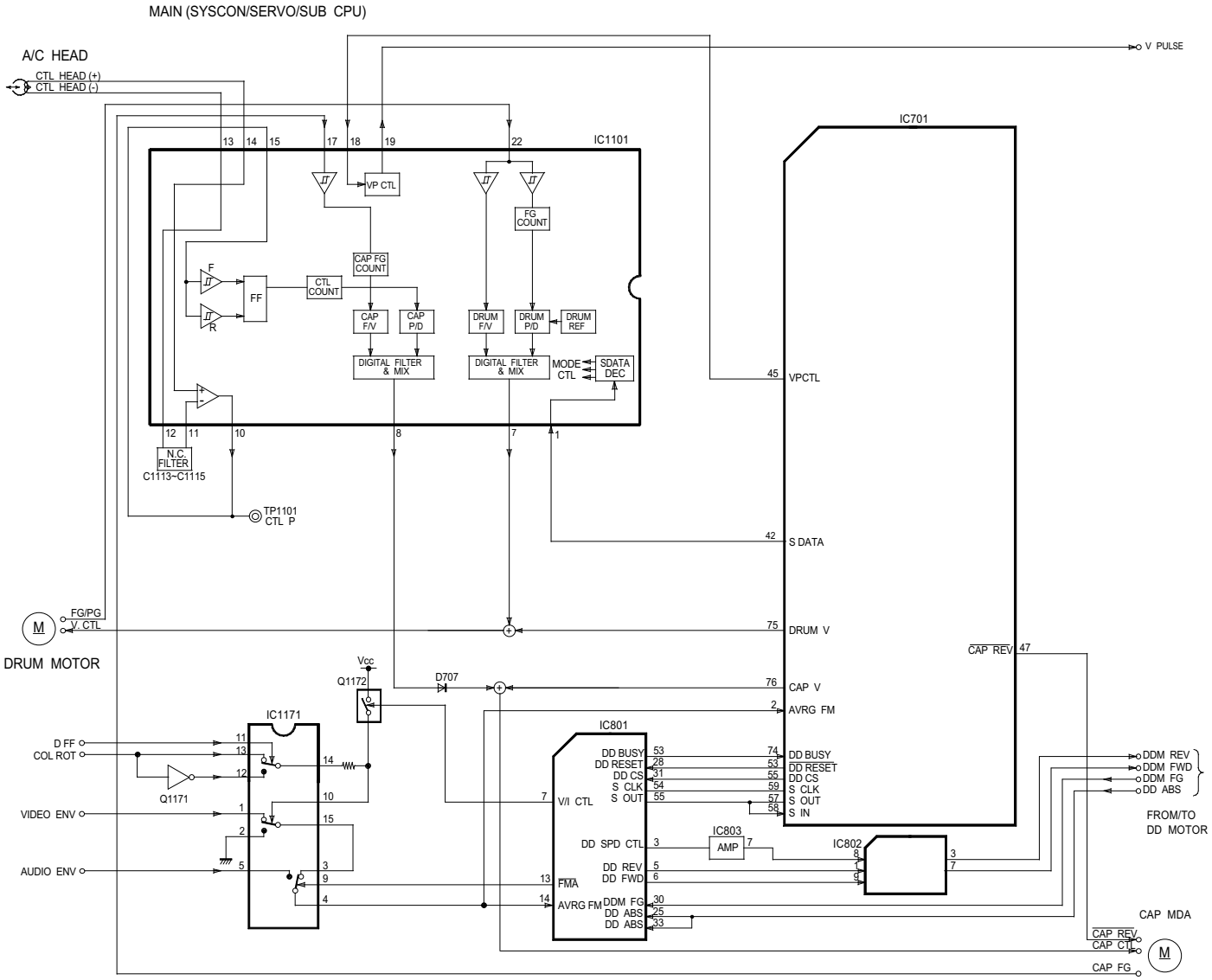


Fig. 2-3-1 System control block diagram

Fig. 2-3-2 shows the DD system control flow chart.

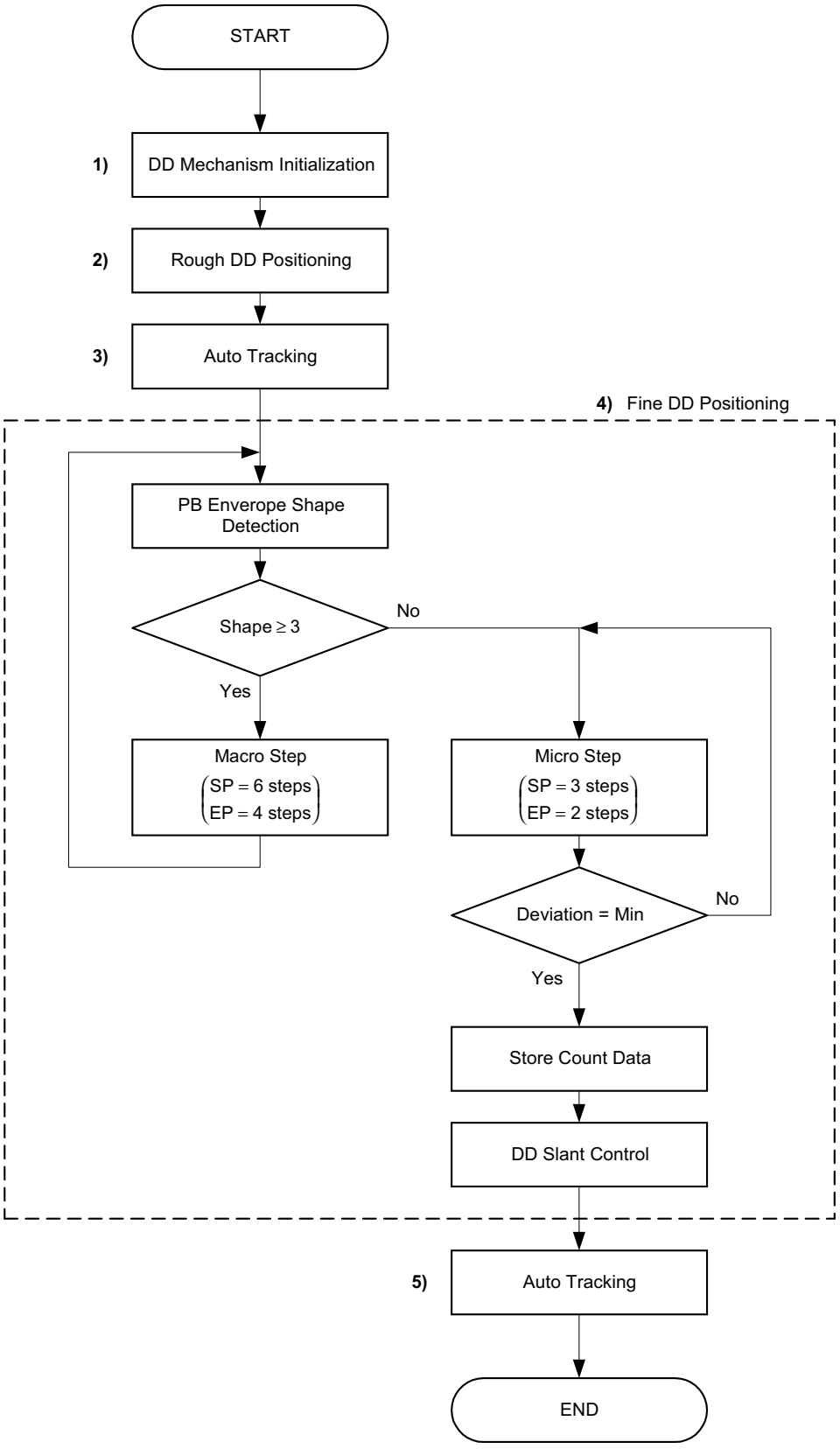


Fig. 2-3-2 DD system control flow chart

The tape speed and pulse count (inclination) are proportional, as indicated in Fig. 2-3-3. The DD operates on this line.

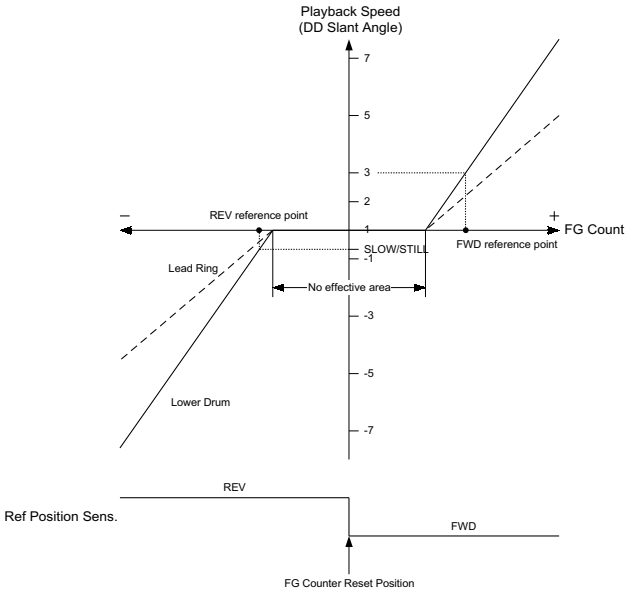


Fig. 2-3-3 Correlation of FG count and search speed

The following description relates to the example of 2× speed in the forward direction (power supply plug connected).

1) DD mechanism initializing

When the power supply plug is connected and IC701 starts, IC701 sends the DD drum initializing command (set inclination for forward direction, ×1 speed) as serial data from pin 57 S OUT to IC801. IC801 pins 6, 5 and 3 respectively control the inclination for direction (DD FWD, DD REV) and speed (DD SPD CTL) by pulse width modulation (PWM). When the drum inclination reaches the initialized position, the change of voltage (low→high, high→low) is applied to pin 33 DD ABS. The drum is then secured at the initialized position.

2) Rough DD position

At the time point drum inclination initializing is complete, if the set is operated for forward 2× speed, the corresponding serial data command is sent from IC701 pin 57 S OUT to IC801. Until DDM FG (pulse frequency proportional to the DD motor rotation) applied to pin 30 reaches the logic 2× forward direction inclination, IC801 controls the drum inclination by DD FWD, DD REV and DD SPD CTL. Although at this point, the drum inclination is generally determined, the inclinations of the head trace and tape track do not completely coincide.

However, IC701 simultaneously sends S DATA from pin 42 to IC1101 for controlling the capstan and drum servos according to the mode.

The above process coarsely adjusts the DD drum head trace position with respect to 2× forward tape track, but these still do not completely coincide. Fine adjustment is therefore conducted as follows.

3) Auto tracking

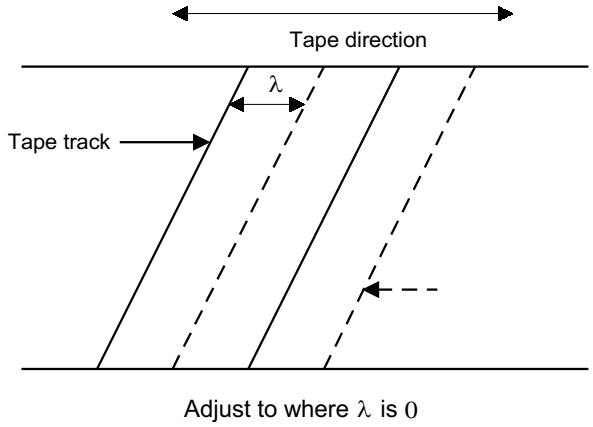


Fig. 2-3-4 Head trace position vs. tape direction

The head trace position is first adjusted with respect to the tape transport direction as indicated in Fig. 2-3-4. In the same manner as normal auto tracking, FMA (Low) at IC801 pin 13 switches the AVRG FM at IC701 pin 2 input envelope signal first to video, then to FMA in sequence.

IC701 averages the FM input in 1 field units and adjusts the tracking point (i.e., head trace position) for the maximum average envelope.

This operation is essentially the same as normal auto tracking.

4) Fine DD Positioning

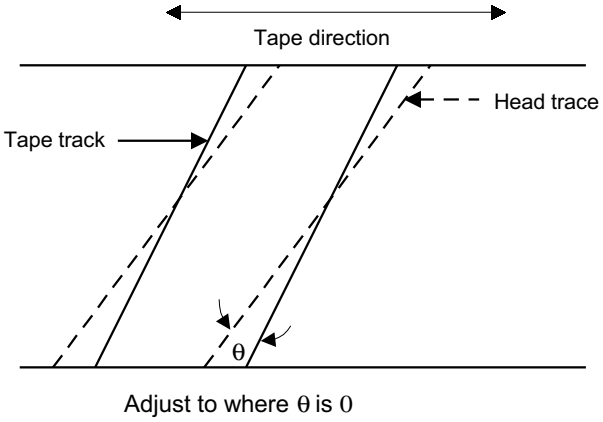


Fig. 2-3-5 Head trace and tape track direction

The head trace direction is then further adjusted to the tape track direction as indicated in Fig. 2-3-5. This has already been approximately adjusted by the process described above.

The fine adjustment process is illustrated in Fig. 2-3-6. The video envelope (video envelope only, not FMA envelope at this time) input at IC801 pin 14 AVRG FM is divided into 6 segments per field. The average value is computed every 1/6th field. The variation is converted into the envelope waveform inclination within one field (repeated for 5 fields to ensure accurate computation). Until the data variation within one field ceases (Detection Result 0 of Fig. 2-3-8), the drum inclination point is detected and the inclination of that point is adjusted.

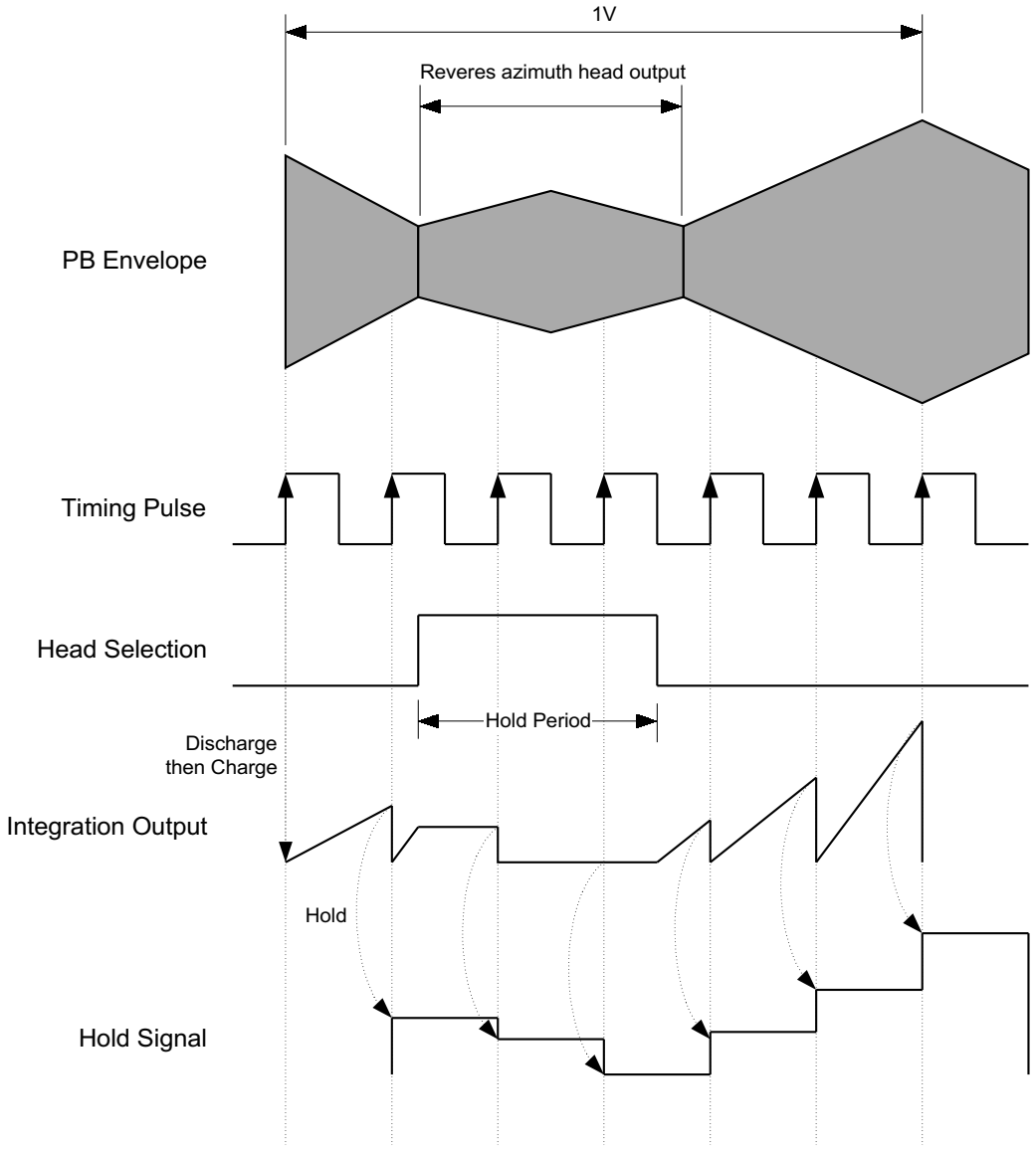


Fig. 2-3-6 Playback envelope detector timing chart

Fig. 2-3-7 shows the Playback envelope shape control flow chart.

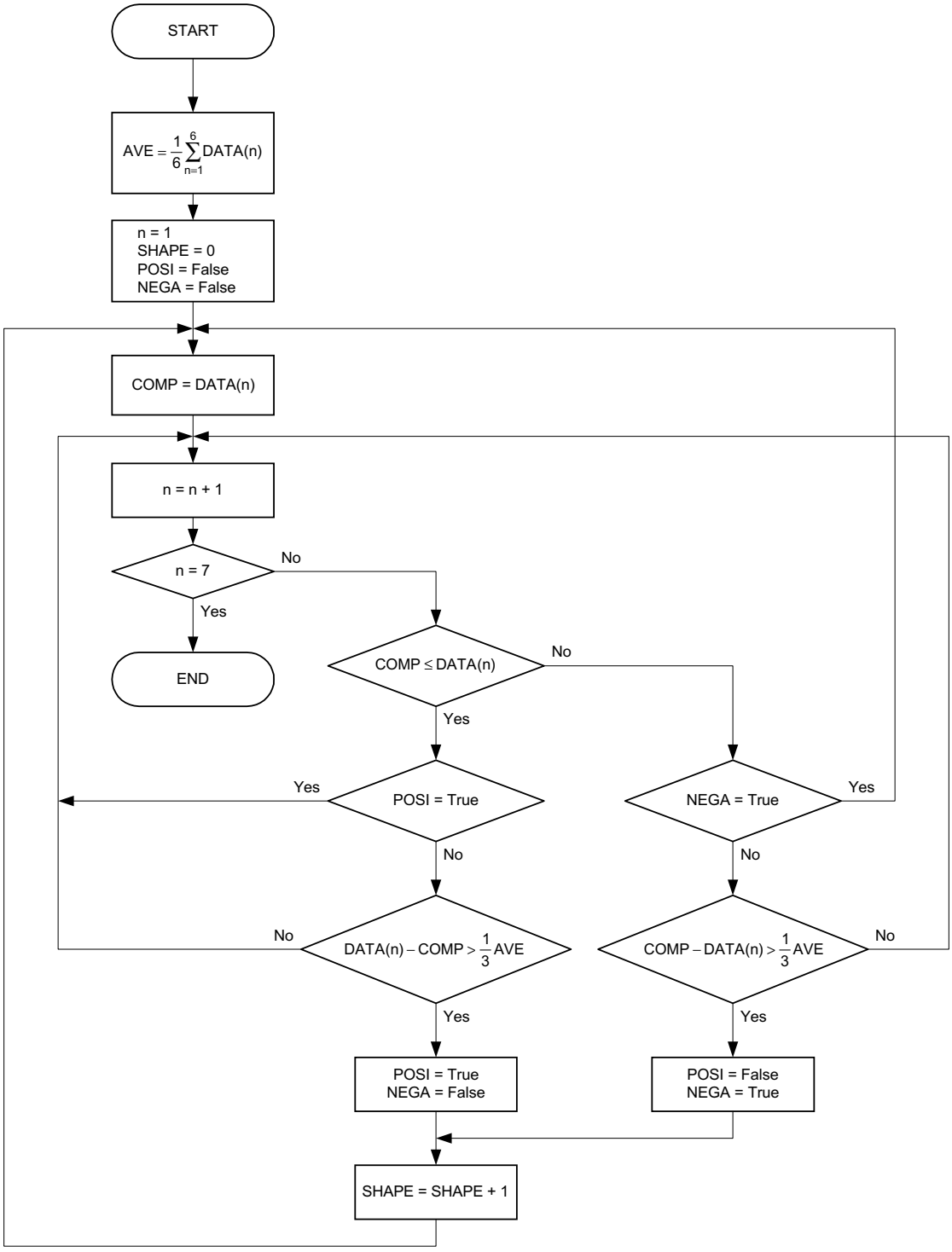


Fig. 2-3-7 PB envelope shape detection flow chart

Fig. 2-3-8 shows the Playback envelope detection results.

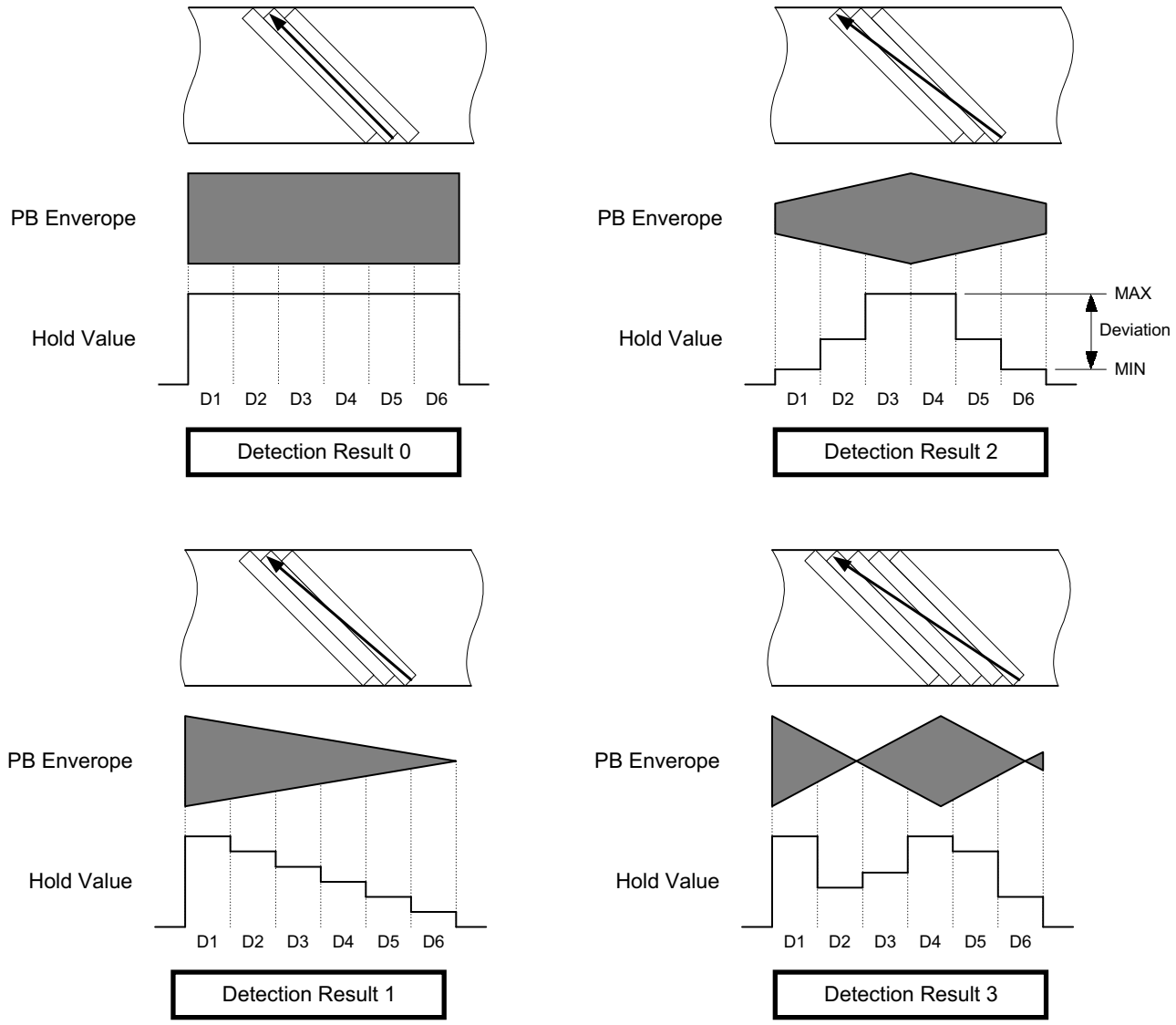


Fig. 2-3-8 Playback envelope detection results

As a result, the head trace direction is precisely aligned with the tape track direction.

5) Auto Tracking

Finally, the normal auto tracking operation of above step 1 is repeated.

Although the 2× forward mode was described by way of example, the same operation is conducted for other modes as well.

2.4 SUB CPU (IC801) PIN FUNCTIONS

Pin No.	Label	IN/OUT	FUNCTION
1	NC	-	Not used
2	SIN	IN	Serial data input (From SYSCON)
3	DDSPDCTL	OUT	DD drum speed control
4	RES.PULSE	OUT	ATFM
5	DDCREV	OUT	DD drum control (reveres)
6	DDCFWD	OUT	DD drum control (forward)
7	V/I CTL(H)	OUT	ATFM integral mode select
8	AVG-FM-CTL	OUT	ATFM integral interval assignment pulse select
9	VSC-CLK	OUT	Serial clock for VSC
10	VSC-DATA	OUT	Serial data output for VSC
11	EE(L)	OUT	EE mode control (L: EE mode)
12	SP(L)	OUT	SP mode control (L: SP mode)
13	FMA(L)	OUT	AT integral FM select (VIDEO: H/FMA: L)
14	AVG-FM	IN	ATFM integral voltage input
15	VREF	IN	Reference voltage
16	NC	-	Not used
17	NC	-	Not used
18	XIN	IN	System clock (8 MHz)
19	XOUT	OUT	System clock (8 MHz)
20	NC	-	Not used
21	AVSS	-	GND (for analog circuit)
22	VSS	-	GND
23	VCC	-	Power supply
24	NC	-	Not used
25	DDABS	IN	DD drum position detect (1): Not used
26	NC	-	Not used
27	NC	-	Not used
28	DD.RESET	IN	Reset pulse (for DD system)
29	NC	-	Not used
30	DD.MFG	IN	DD drum position detect (2)
31	DDCS	IN	Chip select (for DD system)
32	D.FF	IN	Drum rotation detect
33	DDABS	IN	DD drum position detect (1)
34	NC	-	Not used
35	N.REC(H)		Normal audio REC: H, normal audio recording control signal
36	FRONT(H)		Input select : FRONT(H)/OTHER(L), input select control signal
37	NC	-	Not used
38	BEST(L)	OUT	Best system control signal (L: best system on)
39	AS-ATT2		Not used
40	AP ON(L)		PB best on: L
41	P.CTL(H)	OUT	Switching regulator control signal (H: SW Reg. on)
42	AUX(L)	OUT	External input control signal (L: Ext.)
43	AS-ATT1		Not used
44	NC	-	Not used
45	NC	-	Not used
46	CONV CTL(H)	OUT	RF converter control signal (H: RF converter on)
47	COMBSW OFF(L)	OUT	Transition period color improvement signal
48	BIL SELL	OUT	Main/main+sub select signal
49	NC	-	Not used
50	NC	-	Not used
51	VSS	-	Ground
52	NC	-	Not used
53	DD BUSY	OUT	Serial data receive ready signal: L (to SYSCON)
54	S CLK	IN	Serial clock input (from SYSCON)
55	SOUT	OUT	Serial data output (to SYSCON)
56	NC	-	Not used

Table 2-4-1 Sub CPU (IC801) pin functions

2.5 VOICE SPEED CONTROL (VSC) SYSTEM

The dynamic drum (DD) system includes a sound signal processor that operates during search to enable reproducing speech with pitch and tone closely approximating natural voice playback at normal speed. This function operates only for Normal (longitudinal) track recording (since the hi-fi sound is recorded as FM).

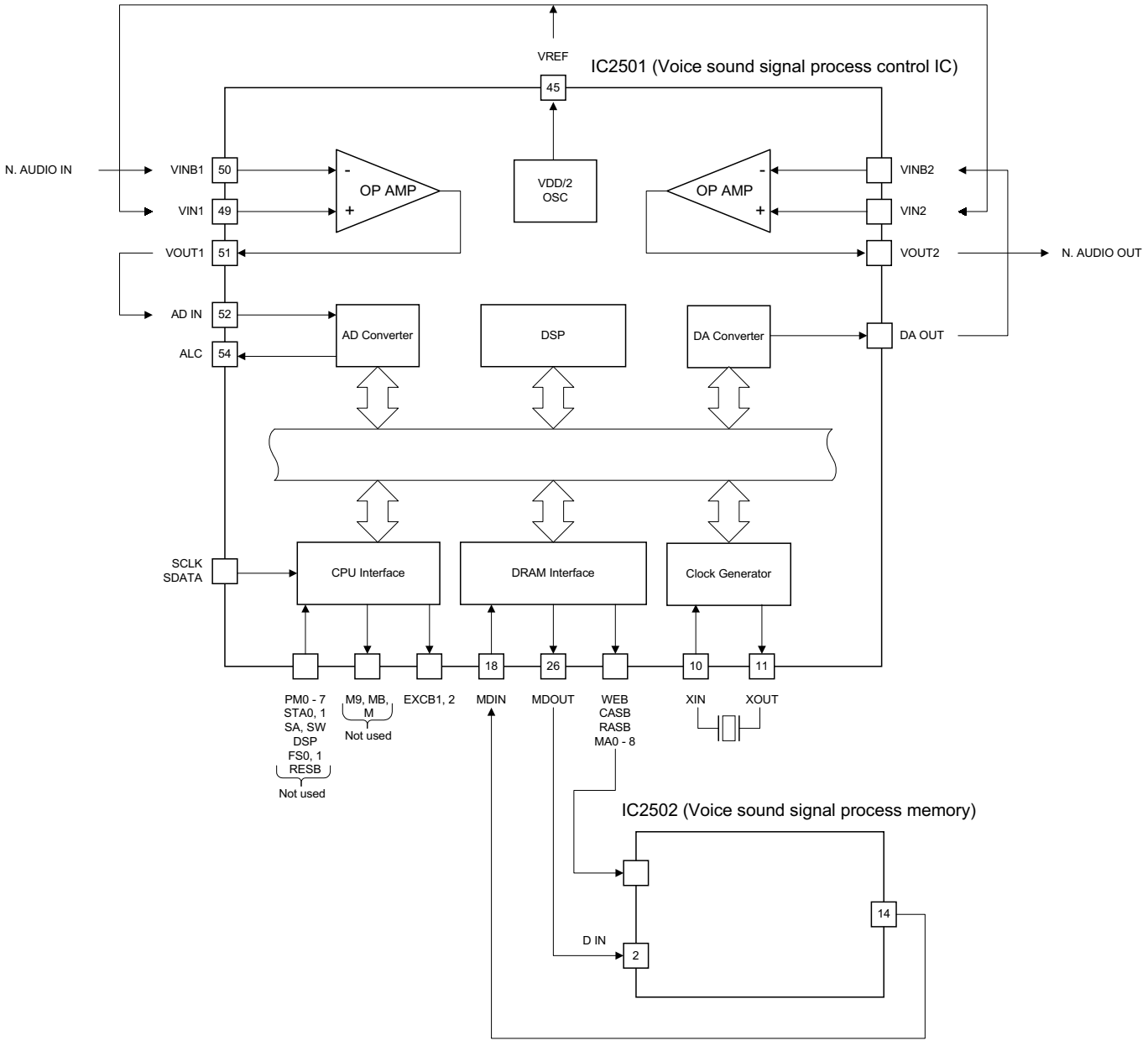


Fig. 2-5-1 VSC system block diagram

Voice signal processing is controlled by IC2501, while IC2502 functions as a process memory. IC2501 controls ic2502 read or write for processing the voice signal. When no process is being conducted for the voice signal, the signal simply goes through IC2501.

Two signal processing methods are used according to the search speed. At the FWD2 speed, time difference adaptive speech rate conversion (DSP) provides precise signal processing. At the 3, 5 and 7 times forward and reverse speeds, somewhat simpler processing is used compared to DSP.

2.5.1 Simple process

As indicated in Fig. 2-5-2, in the simple process mode, part of the input sound is simply discarded to provide a standard speech rate. For example, at speed multiple n, the memory write clock in multiplied 6.4 kHz x n, while the readout clock is fixed at 6.4 kHz. As the figure shows, considerable omissions are produced by this process.

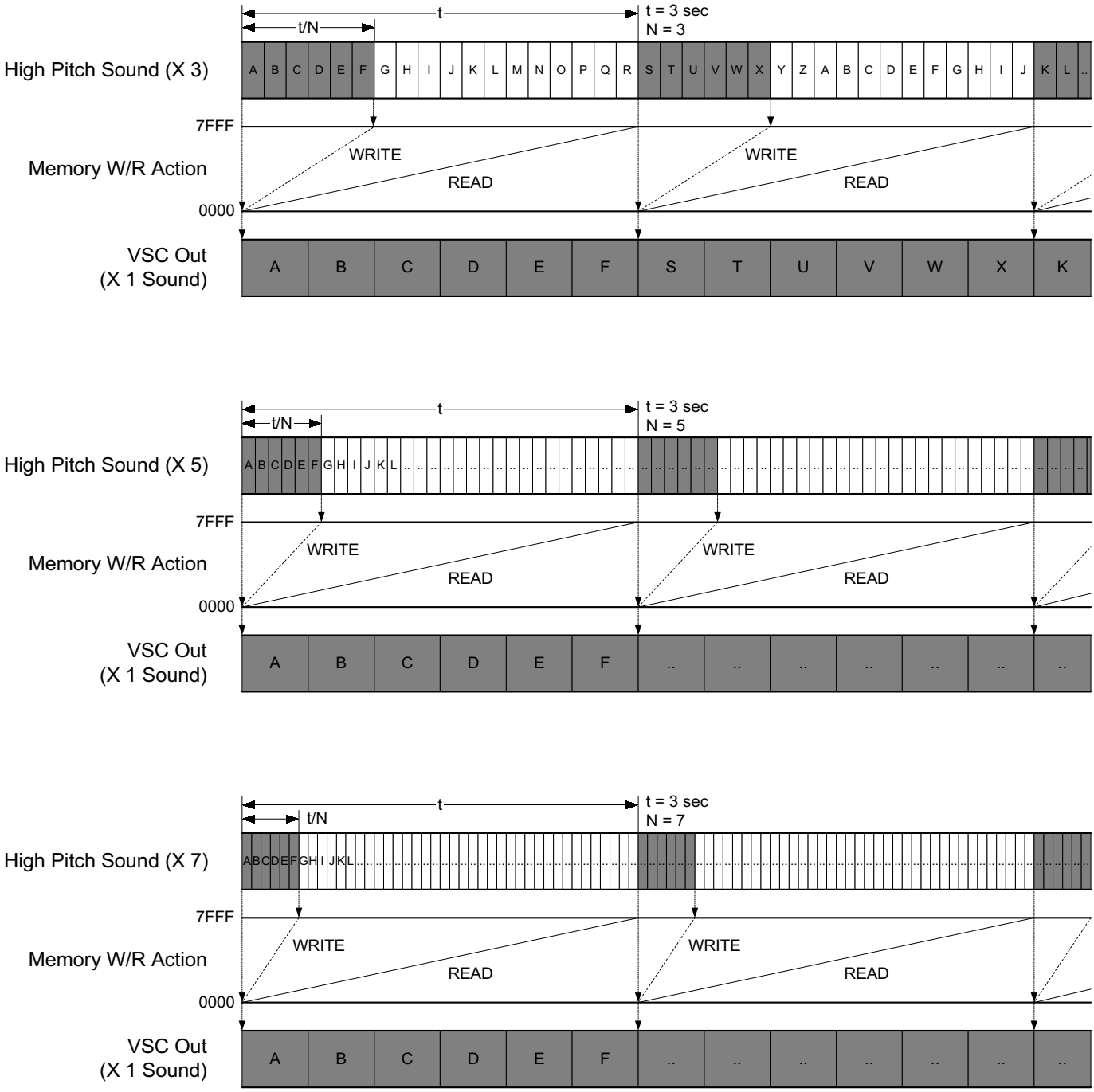
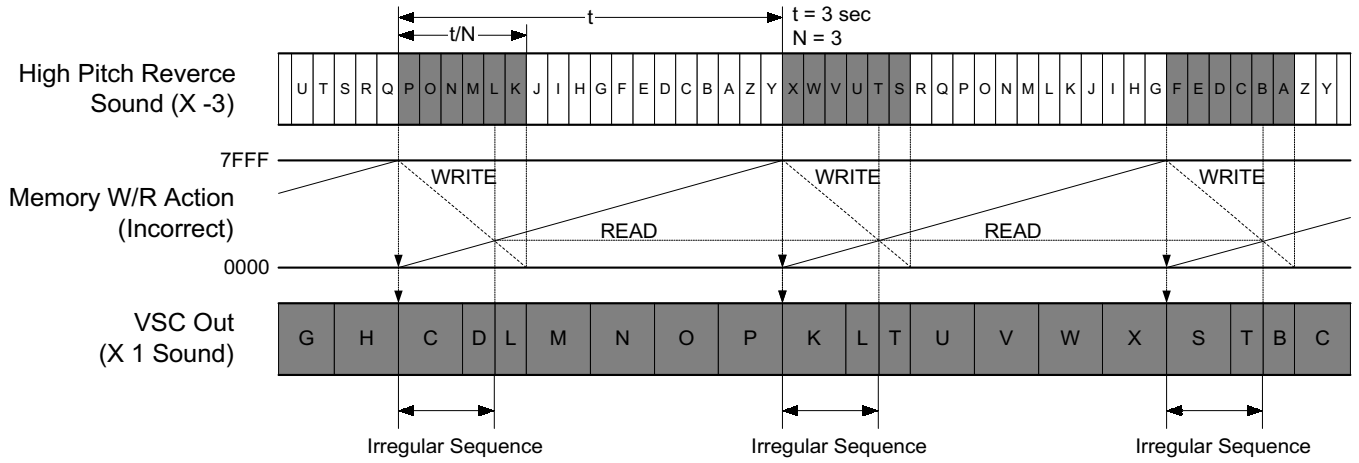
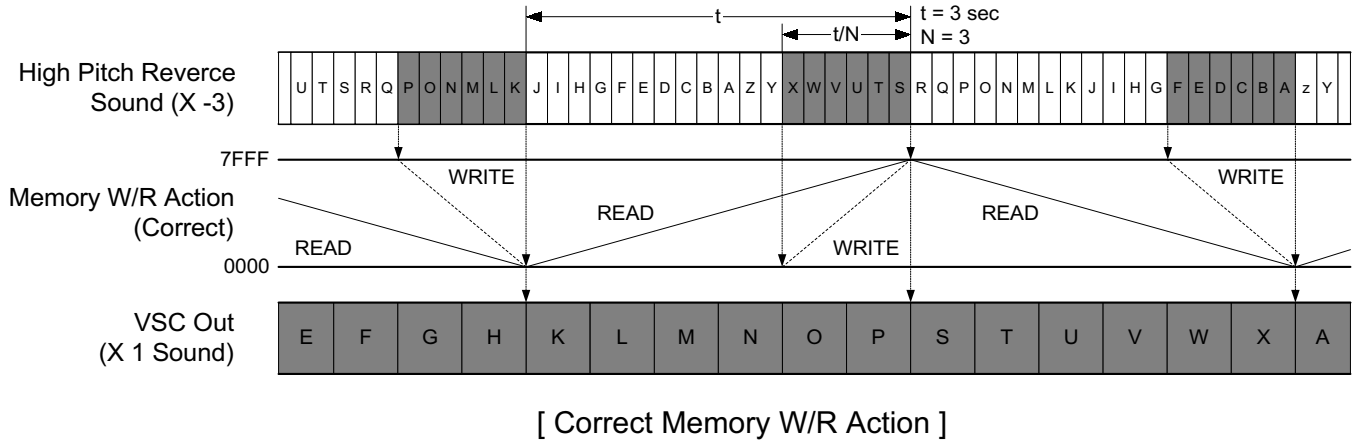


Fig. 2-5-2 Principle of VSC (Search FWD sound)

During reverse playback, part of the reverse input is sampled and converted into normal forward direction speed, as shown in Fig. 2-5-3 and Fig. 2-5-4.



[Incorrect Memory W/R Action]



[Correct Memory W/R Action]

Fig. 2-5-3 Principle of VSC (Search REV sound)

The write and readout clocks are the same as search FWD. The speech quality is also the same as search FWD.

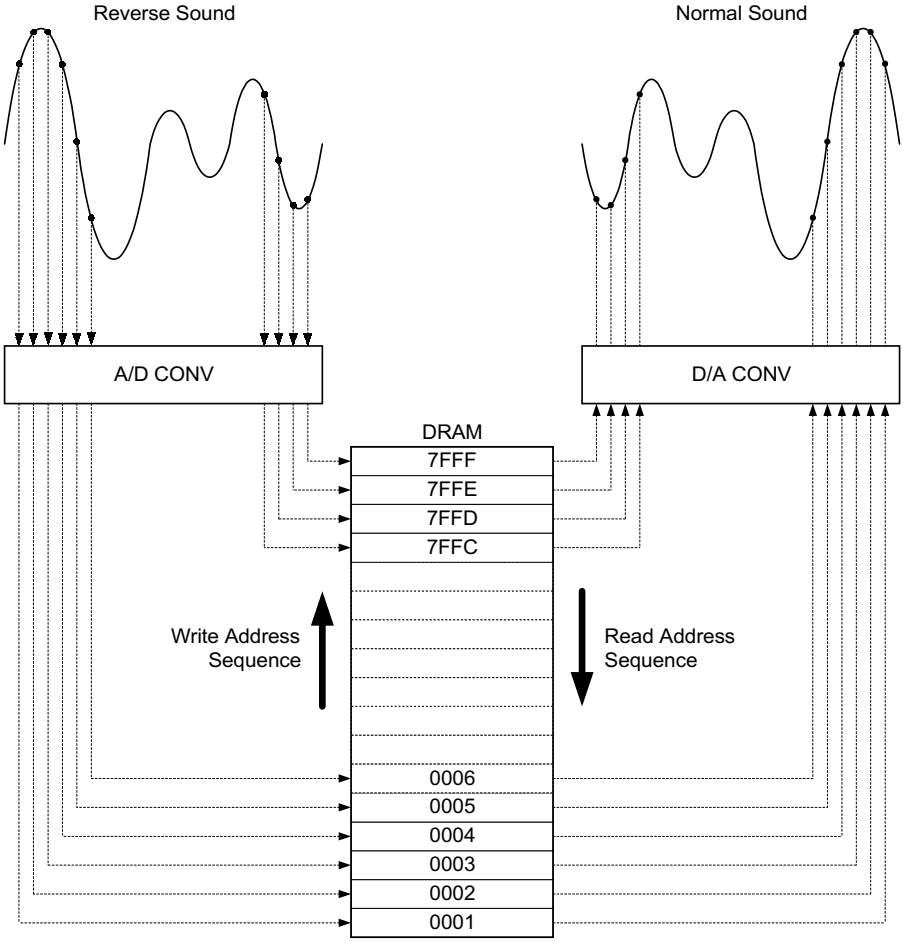


Fig. 2-5-4 Principle of reverse sound restoration

2.5.2 DSP

The processing during forward 2 times playback is described below.
The voice signal is processed in time units of approximately 3 seconds. The processing principle is described as follows.

1) Delete portions without voice

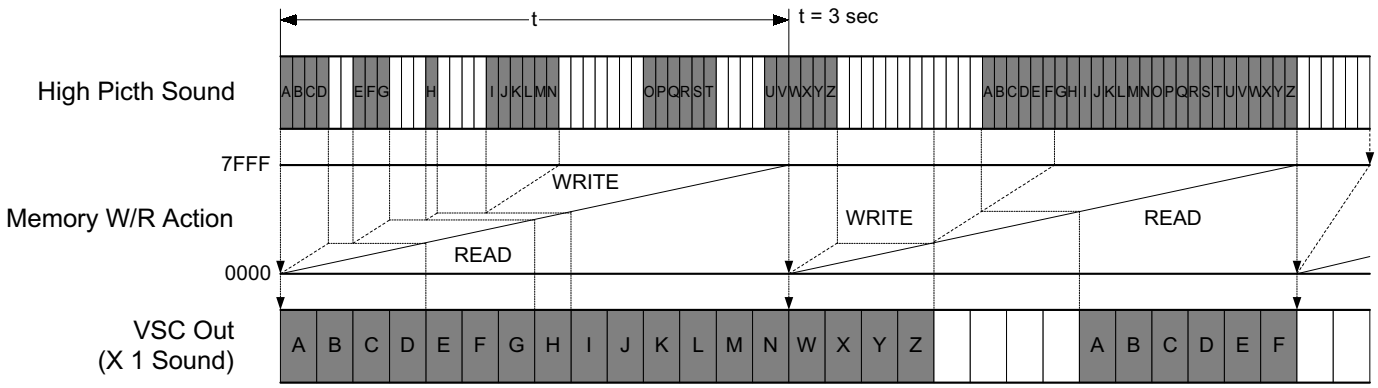


Fig. 2-5-5 Principle of no sound elimination (Search FWD sound)

The first step is to delete the unvoiced components between the spoken words of the original dialog. The sound data components are then written into the processor memory using a 12.8 kHz write clock. Writing is inhibited for unvoiced data components. The amount of data is first reduced in this manner.
However, because of physical sounds, such as ambient noise or background music, there are no portions where sound is truly absent. Therefore, the threshold for determining absence of sound is varied adaptively according to sound conditions in order to distinguish between ambient noise and the desired speech.
During FWD2 times, the threshold between sound and no sound is 1:1. Thus, within the 3 second time unit, the threshold is changed according to the sound status in order to derive a 1.5 second sound component.

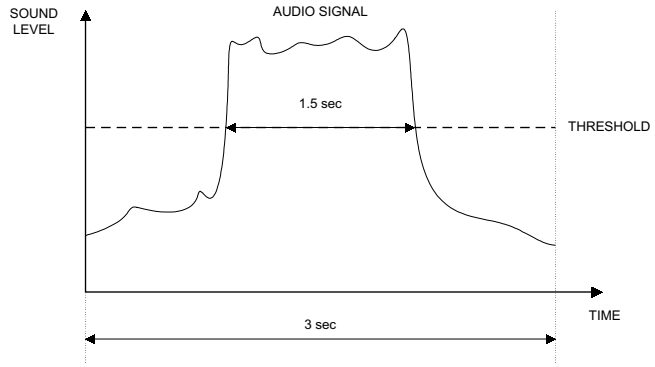


Fig. 2-5-6 Delete portions without voice

As shown in Fig. 2-5-6, the threshold is set in order to obtain a precisely 1.5 second sound component. By setting the voice speed control memory readout clock to 6.4 kHz (12.8 kHz × 1/2), the written data quantity (1/12.8 kHz × 1/2) and readout data quantity 1/6.4 kHz) coincide, thus producing the ideal sound processing state.
Although the written data sound pitch is twice normal, by reading out at 1/2 the clock speed, the sound pitch is also returned to normal. This forms the basic principle of FWD2 times sound processing.

2) Readout clock adjustment

As described above, the ideal detection ratio between presence and absence of sound is 1:1. But in cases such as strongly varying sound or a sudden sound in a quiet scene, the playback sound cannot be reduced to 1/2 by only removing the silent components.

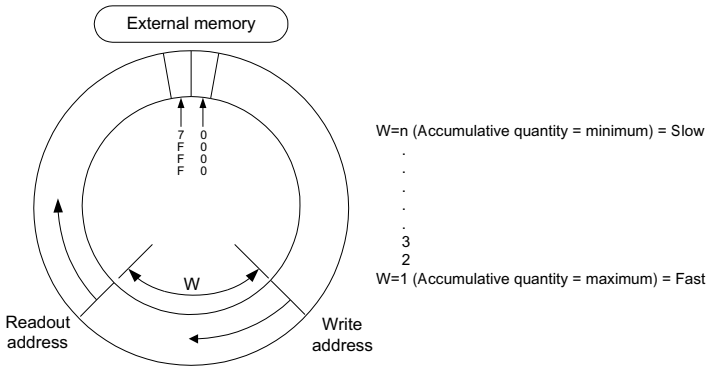


Fig. 2-5-7 Memory (ring memory) principle

As indicated in Fig. 2-5-7, the memory write address must always precede the readout address. By no means can the write address overtake the read address, or the read address overtake the write address. In such events, the readout data become discontinuous and faulty.
The present system incorporates software to set the silent component detection threshold to where the sound component processing time unit does not decline below 1/2 in order to prevent the possibility of the readout address overtaking the write address. However, there is ample possibility of the sound component continuing to where the signal processing time unit exceeds 1/2. In this case, if the readout clock is left at 6.4 kHz, the write address gradually overtakes the readout address.
The following process therefore prevents the write address from overtaking the readout address.
Step 1 is conducted, then if the write address still overtakes the readout address, step 2 is conducted.

(1) The readout clock is speeded by 6.4 kHz x (1 to 1.3).
(2) Write to memory is inhibited.

However, when these steps are necessary, the playback sound pitch is raised slightly and part of the sound is omitted.

2.5.3 Voice speed control IC (IC2501) pin functions

Pin No.	Label	IN/OUT	Function
1	PM0	-	Not used
2	PM1	-	Not used
3	PM2	-	Not used
4	PM3	-	Not used
5	PM4	-	Not used
6	PM5	-	Not used
7	PM6	-	Not used
8	PM7	-	Not used
9	VSS	-	Ground (for digital circuit)
10	XIN	IN	OSC terminal
11	XOUT	OUT	OSC terminal
12	STA0	-	Not used
13	STA1	-	Not used
14	SA	-	Not used
15	SW	-	Not used
16	PAUSE	-	Not used
17	CASB	OUT	Column address strobe output to voice sound signal process memory IC
18	MDDIN	IN	Data input from voice sound signal process memory IC
19	MA3	OUT	Address output to voice sound signal process memory IC
20	MA4	OUT	Address output to voice sound signal process memory IC
21	MA5	OUT	Address output to voice sound signal process memory IC
22	MA6	OUT	Address output to voice sound signal process memory IC
23	MA7	OUT	Address output to voice sound signal process memory IC
24	VDD	-	Power supply (for digital circuit)
25	MA8	OUT	Address output to voice sound signal process memory IC
26	MDOUT	OUT	Data output to voice sound signal process memory IC
27	WEB	OUT	Write enable output to voice sound signal process memory IC
28	RASB	OUT	Row address strobe output to voice sound signal process memory IC
29	MA0	OUT	Address output to voice sound signal process memory IC
30	MA1	OUT	Address output to voice sound signal process memory IC
31	MA2	OUT	Address output to voice sound signal process memory IC
32	NC5	-	Not used
33	SCLK	IN	Serial interface clock input
34	SDATA	IN	Serial interface data input
35	DSP	-	Not used
36	M9	-	Not used
37	M8	-	Not used
38	FS0	-	Not used
39	FS1	-	Not used
40	NC4	-	Not used
41	VSS	-	Ground (for digital circuit)
42	M	-	Not used
43	DAOUT	OUT	DA converter output
44	VSSA	-	Ground (for analog circuit)
45	VREF	OUT	Reference voltage (VDD/2)
46	VIN2	IN	Internal OP. amp. 2 non-inverted input
47	VINB2	IN	Internal OP. amp. 2 inverted input
48	VOUT2	OUT	Internal OP. amp. 2 output
49	VIN1	IN	Internal OP. amp. 1 non-inverted input
50	VINB1	IN	Internal OP. amp. 1 inverted input
51	VOUT1	OUT	Internal OP. amp. 1 output
52	ADIN	IN	AD converter input
53	VDDA	-	Power supply (for analog circuit)
54	ALC	-	AD converter overflow signal output
55	NC1	-	Not used
56	NC2	-	Not used
57	NC3	-	Not used
58	RESB	IN	System reset
59	VDD	-	Power supply (for digital circuit)
60	EXCB2	OUT	Signal enforce data EXCB output
61	EXCB1	OUT	Signal enforce data EXCB output
62	NC0	-	Not used
63	TST1	-	Not used
64	TST0	-	Not used

Table 2-5-1 Voice speed control IC (IC2501) pin functions

SECTION 3
VIDEO PROCESSING

This section is experience for HR-VP830U as an example.
A new signal processor IC (audio/video chip) is used in the video system. The IC automates the pre/rec and video circuit adjustments previously required when replacing the heads, and uses a new system for color signal down conversion.
These functions are described below.

3.1 BEST SYSTEM

Best system refers to combined auto calibration during recording and auto picture during playback. The system eliminates the previous need for pre/rec and video circuit adjustments when replacing the heads and reduces picture quality degradation arising from video recording and playback response changes due to head wear.

1) Auto calibration
The optimum recording current and detail enhancement are set automatically during recording.

2) Auto picture
Video frequency response and noise cancelling are set automatically during playback.

3.1.1 Auto calibration system

1) Process
Fig. 3-1-1 indicates the auto calibration system process, while Fig. 3-1-2 indicates the timing chart.

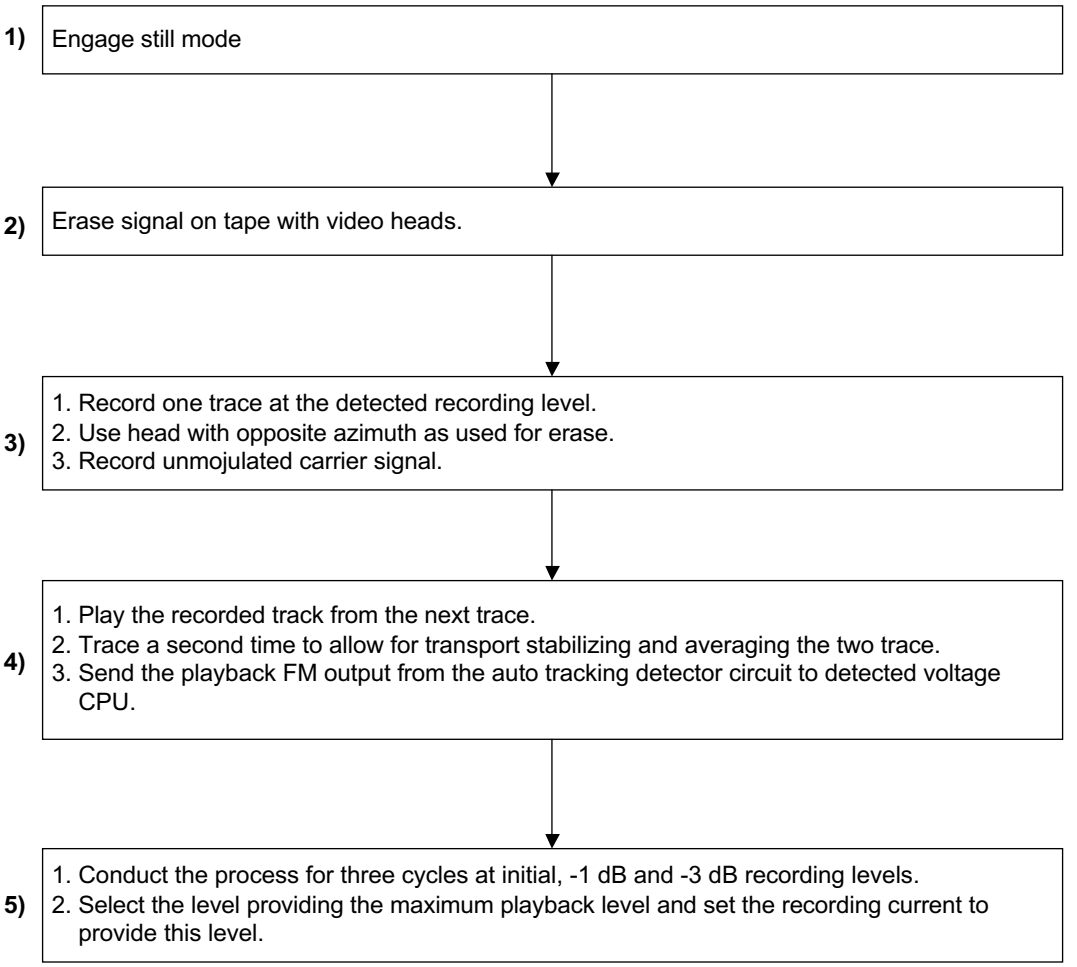


Fig. 3-1-1 Auto calibration system process

•Auto calibration system timing chart

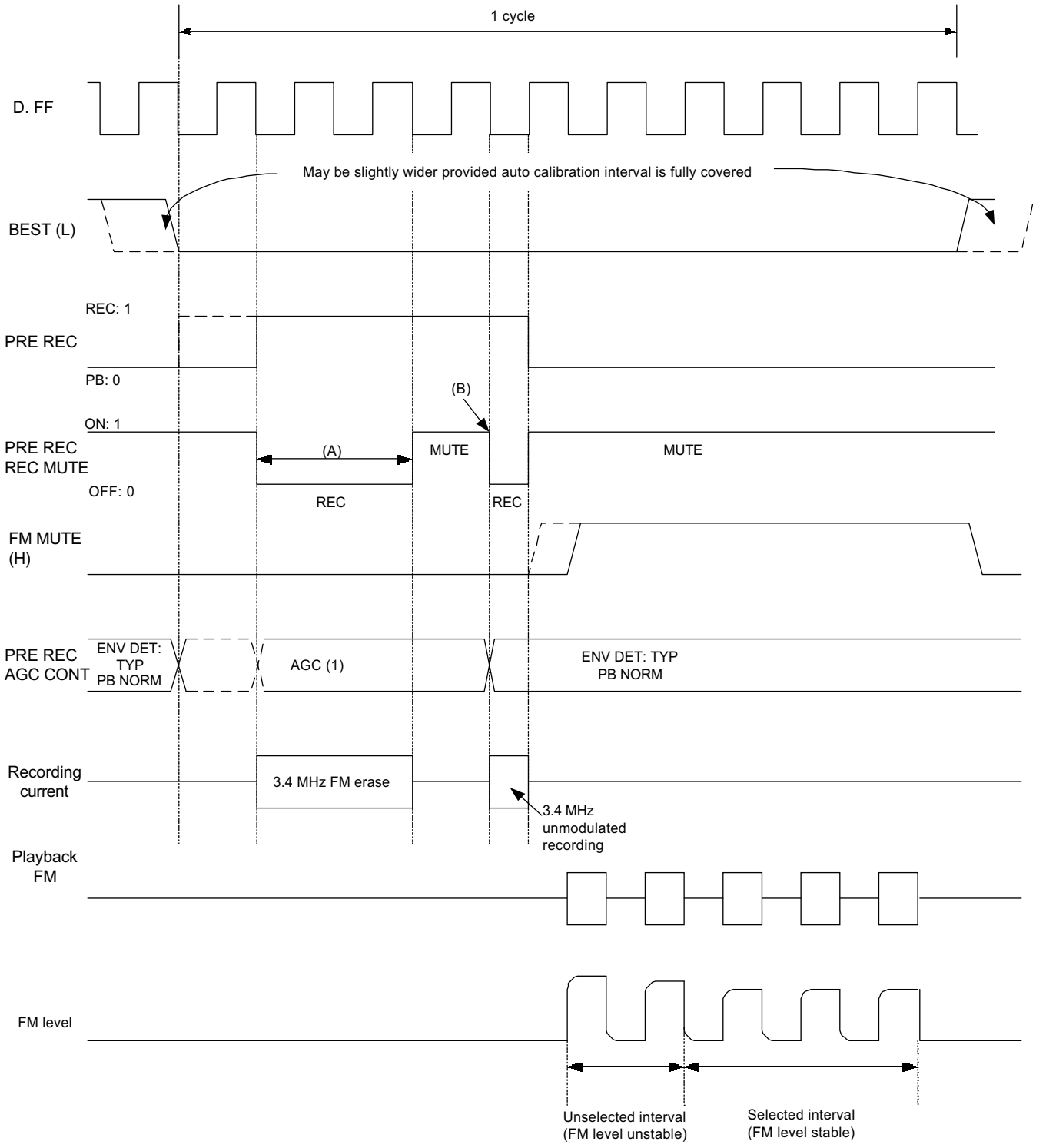


Fig. 3-1-2 Auto calibration system timing chart (SP mode)

2) Auto calibration operating states
(1) Normal recording
Once each for SP and EP modes when shifting from Stop to REC or REC Pause. Auto calibration is conducted only when selecting the tape speed (SP or EP).

(2) Timer recording
At the first timer REC program, conducted for both SP and EP modes during timer standby REC Pause.

3) Auto calibration reset
(1) When cassette tape is removed.

(2) When power outtage backup is depleted.

4) Detail enhancer (DE) effect
The detail enhancer effect is increased for the SP mode and decreased for the EP mode.

3.1.2 Auto picture system

1) Operation
The auto picture system process is indicated in Fig. 3-1-3.

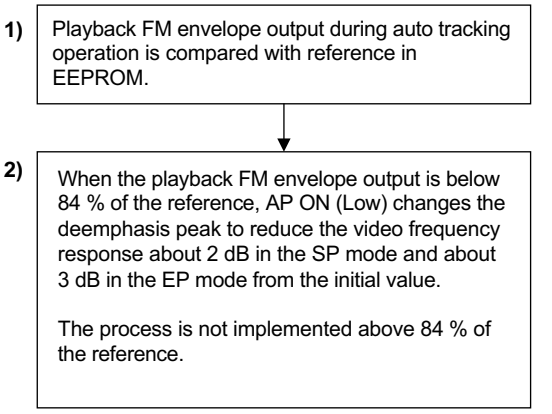


Fig. 3-1-3 Auto picture system operation

2) Operating state
Only after completion of auto tracking operation.

3) Reset conditions (both SP and EP)
(1) When cassette tape is removed.

(2) When power outtage backup is depleted.

4) Reference write to EEPROM
As can be noted from the operation, the system requires a reference for determining the size of the playback FM envelope. The reference must therefore be entered beforehand in the EEPROM whenever the heads are replaced. The procedure is as follows.
(1) Record and playback a test pattern signal with a standard tape (SP and EP).

(2) During playback send L from the adjustment remote controller (SP and EP).

(3) At completion of entry, automatically Stop.

5) Noise canceller (NC) depth
The noise canceller effect is shallower in the SP mode and deeper in the EP mode.

3.1.3 Best system control

The Fig. 3-1-4 block diagram illustrates the best system control signal flow.

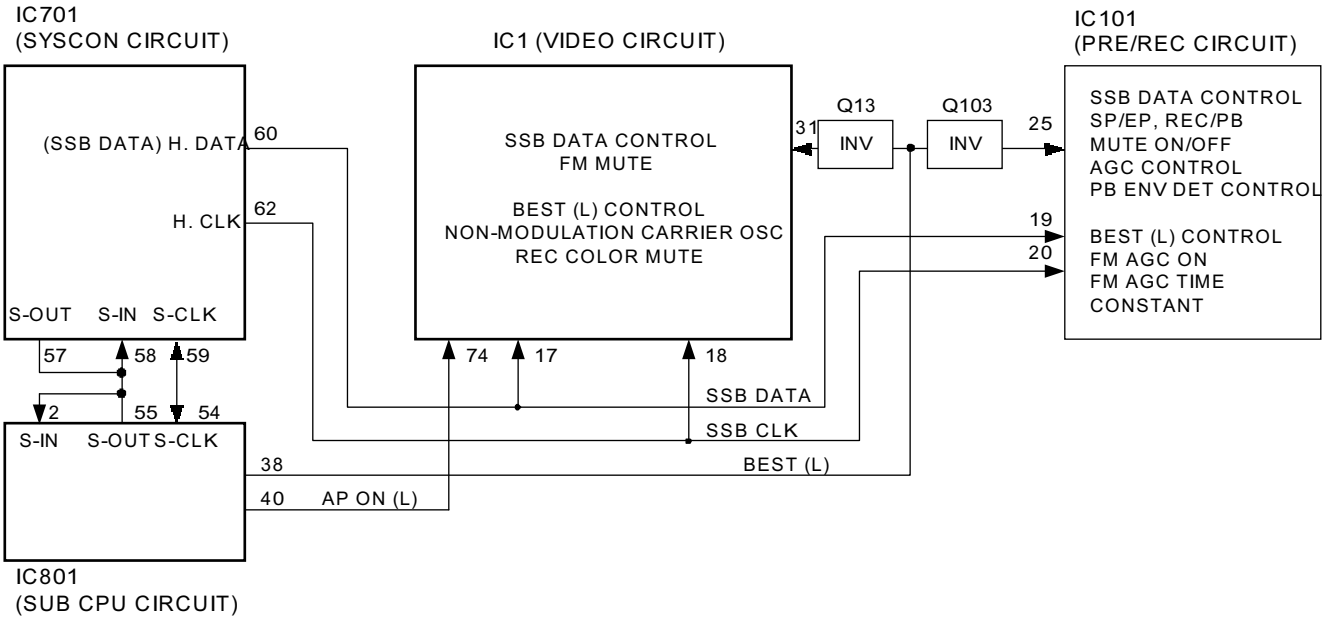


Fig. 3-1-4 Control signal block diagram

IC701 is the main system control (syscon) IC. Although IC801 functions mainly for DD drum system control, an IC701 expander function is also included. These two ICs control the video IC1 and pre/rec IC101 circuits.
Table 3-1-1 summarizes the IC1 and IC101 control functions of SSB data and BEST (Low) in the best system.

Circuit	Control signal	Operation
PRE/REC (IC101)	SSB data	SP/EP, REC/PB switching Mute on AGC and PB ENV DET setting
	BEST (L)	Time constant selection during FM AGC on
VIDEO (IC1)	SSB data	FM mute on
	BEST (L)	Unmodulated carrier oscillator on Recording color mute on

Table 3-1-1 SSB data and BEST (Low) control

As can be noted from the table, during best system operation, SSB data provide various selections and settings at IC101. BEST (Low) speeds the time constant when FM AGC is always on. Since recording current setting is in one track units, FM AGC operation is impracticable with ordinary time constants.
The SSB data set the FM mute at IC1. IC1 is in the EE mode during recording current setting. Without FM mute, REC FM would interfere with the playback calibration signal for setting the recording current and prevent accurate level detection.
BEST (Low) engages recording color mute during unmodulated carrier oscillation.

3.2 DOUBLE MAIN CONVERTER

Fig. 3-2-1 shows a block diagram of a typical playback color signal processor.

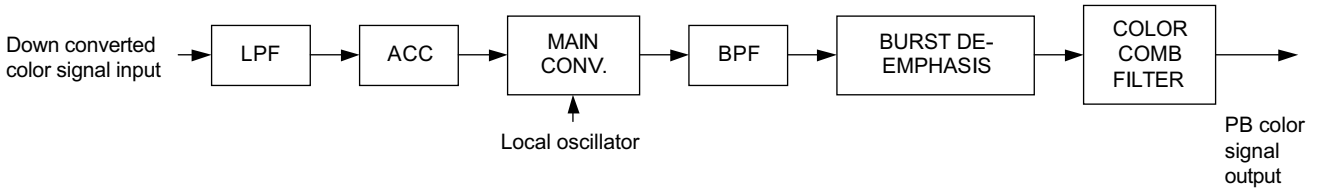


Fig. 3-2-1 PB color processor

1) Conventional main converter

Consumer type video tape recorders, including formats other than VHS, convert the color signal to lowband prior to recording in order to compress the video signal recording bandwidth and reduce phase jitter in the playback color signal. Converting the color signal to lowband for recording and demodulation during playback are functions of the main converter circuit. The main converter is a type of multiplier and functions to align the input and local oscillator signals,

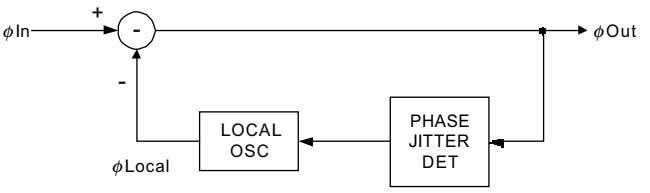


Fig. 3-2-2 Playback APC loop block diagram

The playback automatic phase control (APC) loop is composed as indicated in Fig. 3-2-2. Assume, for example, the input phase jitter *f* In goes directly to the output. This is detected by the phase jitter detector, which operates to equalize *f* Local of the local oscillator output to *f* In. The phase subtract function of the main converter then cancels *f* In with *f* Local to eliminate the phase jitter. This forms the principle of jitter correction by the APC loop.

2) Conventional color comb filter

A phase shift (PS) system is used for recording in the VHS format for reducing crosstalk between adjacent color signal tracks. The principle of this system is outlined in Fig. 3-2-3. The phase of the down converted color signal for recording is rotated 90 degrees every horizontal line (1 H) so that the mutual rotation of adjacent tracks is opposite. The phase is rotated by rotating the phase of the local oscillator signal aligned at the main converter.

During playback, as indicated in Fig. 3-2-4, the color comb filter returns the original phase and by synthesizing with the 1 H previous signal, the crosstalk component is canceled.

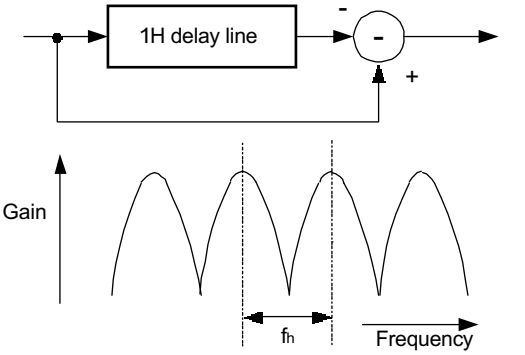


Fig. 3-2-4 Color comb filter

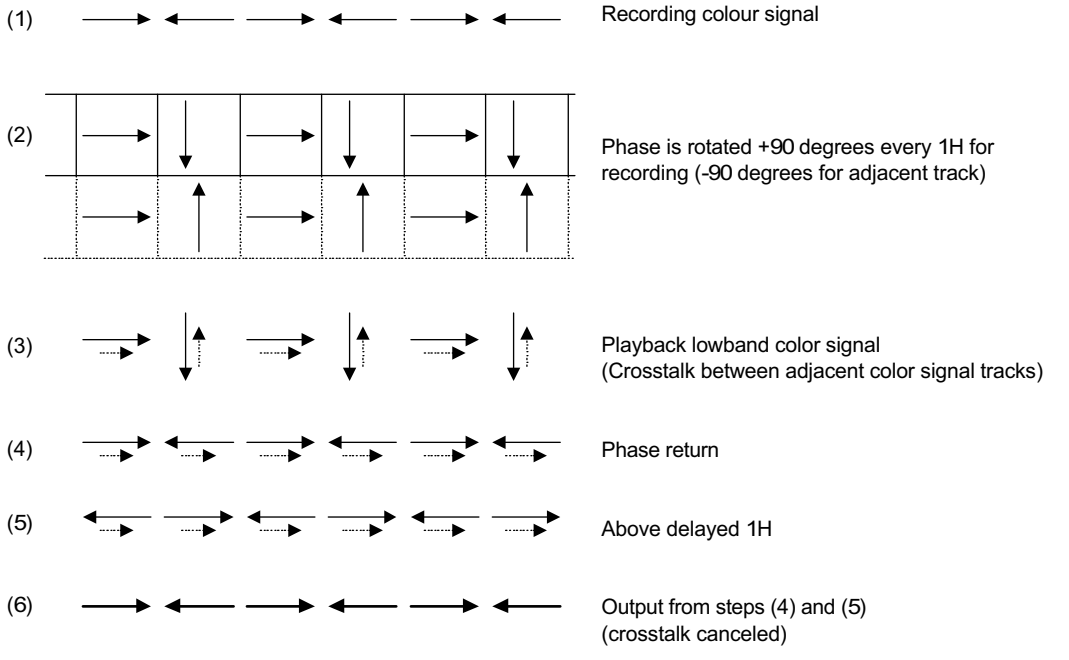


Fig. 3-2-3 Phase shift principle

3) Double main converter outline

Fig. 3-2-5 illustrates signal processing by the new double main converter circuit.

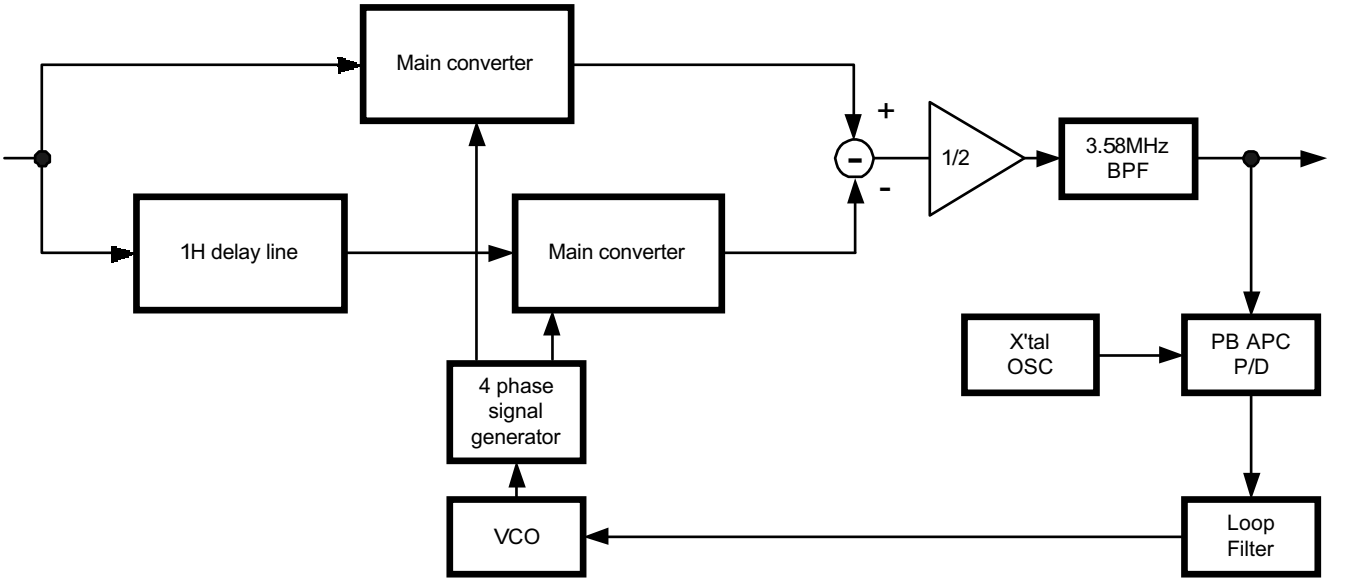


Fig. 3-2-5 Double main converter signal processing

In the conventional playback system, after demodulation of the down converted color signal at the main converter, crosstalk is reduced by the comb filter. The new system uses two main converters for simultaneous demodulation and crosstalk reduction.

The color signal jitter component is also removed by the system indicated in Fig. 3-2-6.

By utilizing this system, the multistage fast clock delay line used in the previous comb filter (due to the wide bandwidth of the demodulated color signal) is no longer required for removing crosstalk, thus allowing a simpler circuit and cost economy.

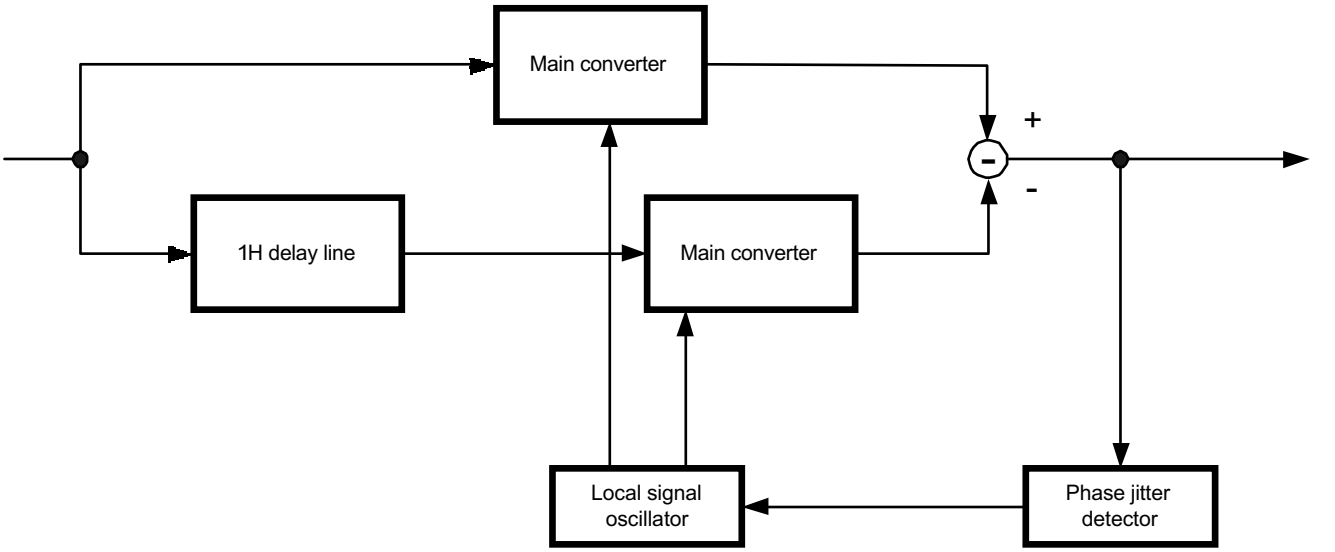


Fig. 3-2-6 Jitter removal with double main converter

3.3 IC (AUDIO/VIDEO 1 CHIP) PIN FUNCTIONS

3.3.1 IC1 (AV 1 chip) pin functions (1/2)

Pin No.	Label	In/Out	Function
1	P-EQ f_0/Q ADJ2	-	PB FM signal thermal response adjust
2	G-EQ Q ADJ	-	PB FM signal peaking response adjust
3	f_0/DEV S-DET	-	RE FM MOD frequency deviation filter
4	PB FM IN	IN	PB FM input
5	EDT	-	MESECAM detect filter
6	REC FM OUT	OUT	Recording FM output
7	PB C.IN	IN	PB color (FM) input
8	RESPONSE TYP C COMB DE	-	Not used
9	SW21 CONTROL	-	Not used
10	MESECAM DETECT TRAP	-	Comprises MESECAM and S detect filter
11	C CCD DRIVE	OUT	Color CCD drive
12	LEVEL DET	-	CCD gain adjust
13	C CCD FB IN	IN	Color CCD feedback input
14	C/AUDIO V_{CC}	-	Color and audio system Vcc
15	REC C OUT	OUT	Recording color output
16	SW30 / 25	IN	Low: channel 1, High: channel 2
17	SSB DATA	IN	Serial data input
18	SSB CLK	IN	Serial control clock input
19	CCD CONT	OUT	CCD mode control NTSC
20	DISCRI	-	Disk filter volume
21	LC VCO	-	Inductance for LC VCO oscillation
22	PB APC / REC AFC	-	Playback APC/recording AFC filter
23	CR DET	-	CR non-adjust filter
24	$2F_{SC}$ OUT	OUT	Clock output for CCD
25	C GND	-	Color system ground
26	3.58X'tal IN	IN	Crystal oscillator input for 3.58 NTSC
27	REC APC	-	Recording APC filter connection
28	X'tal OSC OUT	OUT	Crystal oscillator drive
29	ACC DET	-	Burst ACC detect filter
30	4.43X'tal IN	-	Crystal oscillator input for 4.43 (not used)
31	CK DET	-	Color killer detect filter
32	AUDIO BIAS CONT	-	Audio recording bias current control (not used)
33	AUDIO BIAS FILTER	-	Audio recording bias current level adjust
34	AUDIO REC OUT	OUT	Audio recording output
35	AUDIO REC EP SW	-	Audio recording equalization select
36	AUDIO REC IN(-)	-	Audio recording equalization amplifier feedback
37	AUDIO PB EP SW	-	Audio playback equalization select
38	AUDIO PB IN(+)	IN	Audio playback equalization amplifier input
39	AUDIO PB IN(-)	-	Audio playback equalization amplifier feedback
40	AUDIO PB EQ OUT	-	Output for audio playback equalization amplifier feedback

Table 3-3-1 IC1 pin functions (1/2)

•IC1 (AV 1 chip) pin functions (2/2)

Pin No.	Label	In/Out	Function
41	AUDIO ALC FILTER	-	Audio ALC filter
42	AUDIO LINE IN 2	IN	Audio line input 2
43	AUDIO LINE IN 1	IN	Audio line input 1
44	AUDIO BYPASS	-	Bypass capacitor for audio ALC DC restoration
45	AUDIO SEARCH OUT	OUT	Mute output
46	AUDIO LINE OUT	OUT	Audio line output
47	AUDIO GND	-	Audio ground
48	UNCORRELATED OUTPUT	OUT	Uncorrelated signal output
49	KILLER/DC OUTPUT	OUT	Color killer/DC output
50	PB C.OUT	OUT	Playback color output and control for pins 48 and 49
51	B.G.	-	Reference bias filter
52	AUDIO MUTE	-	Hi: line + Rec, Mid: Rec, Lo: mute off
53	SYNC SEP OUT	OUT	Sync separation output
54	Y-V_{CC}	-	Luminance system Vcc
55	COLOR IN	IN	Playback color mixer input
56	SQUELCH	IN	Synthesized V cancel
57	VIDEO OUT	OUT	Electric-to-electric and playback video output
58	VIDEO OUT F.B.C.	-	FBC filter
59	AGC DET	-	Video AGC detect filter
60	LINE(2) IN	IN	Line tuner video input
61	LINE(1) IN	IN	Line tuner video input
62	P CONT	-	Picture control (ground: soft, 3.5 V: hard, open: off)
63	FROM Y-CCD	IN	Y-CCD feedback lowpass filter input
64	VIDEO OUT ALC	-	Video output level non-adjust filter
65	Y-CCD LPF OUT	OUT	Y-CCD lowpass filter output
66	Y-CCD CLAMP	IN	Y-CCD lowpass filter clamp input
67	CCD ADJ	-	CCD gain correction filter
68	Y-CCD DRIVE	OUT	Y-CCD drive output
69	P-EQ f_0/Q ADJ1	-	Playback FM thermal response adjust
70	MAIN CLAMP IN	IN	Main clamp input
71	CLAMP DRIVE	OUT	Y signal transmission route
72	ME ALL/PB FM AGC	-	Main emphasis/playback FM level adjust filter
73	Y.GND	-	Luminance system ground
74	E-PEAK	-	Main deemphasis peaking adjust
75	S-VHS/VHS DETECT	OUT	Hi: S-VHS/Lo: VHS
76	REC FM PBC/PB APL	-	REC: main emphasis FBC filter, PB: main deemphasis ALC filter
77	MAIN EM NF/MAIN DEEM OUT	IN	REC: main emphasis FB input, PB: main deemphasis filter output
78	MAIN EM NF/MAIN DEEM IN	OUT	REC: main emphasis output, PB: main deemphasis filter drive
79	EDGE DO DET	-	Edge D0 detect integration filter
80	G-EQ SB ADJ	-	FM signal low frequency response adjust

Table 3-3-1 IC1 pin functions (2/2)

3.4 IC1 INTERNAL OPERATION

The internal block diagram of IC1 is shown in Fig. 3-4-1. Table 3-4-1 indicates the operations with respect to reference numbers noted in the figure.

3.4.1 IC1 internal block diagram

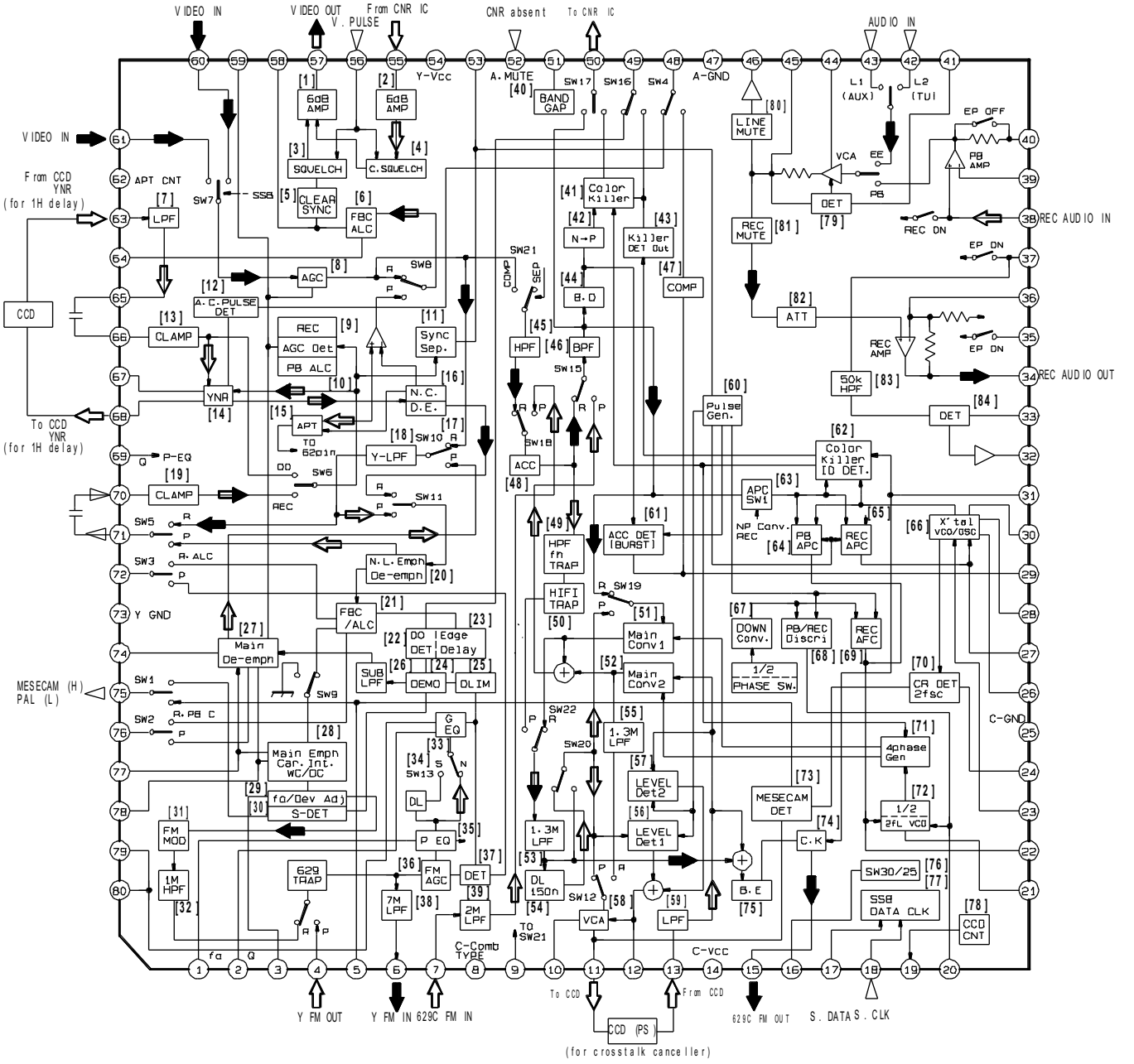


Fig. 3-4-1 IC1 internal block diagram

3.4.2 IC1 operations (1/2)

No	Block name	Operation	Processing signals
1	6dB AMP	6 dB (approx. 2x) amplifier	PB. C
2	6dB AMP	6 dB (approx. 2x) amplifier	PB. C, PB. Y
3	SQUELCH	Special PB V cancel (external control)	PB. Y
4	C.SQUELCH	Mute during REC (EE)	PB. C
5	CLEAR SYNC	Improve sync S/N	PB. Y
6	FBC/ALC	Feedback type auto level adjust	PB. Y
7	LPF	Lowpass filter (2 fsc trap)	PB. Y
8	AGC	Automatic gain control	REC. Y
9	REC AGC DET	REC AGC detect	REC. Y
10	PB ALC	Playback automatic level control	PB. Y
11	SYNC SEP	Sync signal separation	REC. Y, PB. Y
12	A.C PULSE DET	Uncorrelated signal detect (used for YNR)	REC. Y, PB. Y
13	CLAMP	DC level adjust	PB. Y
14	YNR	Y signal noise reduction (active type)	PB. Y
15	APT	Aperture correction	REC. Y, PB. Y
16	N.C.	Noise canceller	PB. Y
17	D.E.	Detail enhancer (high frequency enhancer)	REC. Y
18	Y-LPF	Lowpass filter (3 MHz)	REC. Y, PB. Y
19	CLAMP	DC level adjust	REC. Y, PB. Y
20	N.L.EMPH/DE-EMPH	REC: non-linear emphasis, PB: non-linear deemphasis	REC. Y, PB. Y
21	FBC/ALC	Feedback auto level adjust	REC. Y
22	DO DET	Dropout detect	PB. Y
23	EDGE DELAY	Timing adjust when dropout compensator released	PB. Y
24	D LIM	FM signal limiter	PB. Y
25	DEMO	FM demodulator	PB. Y
26	SUB LPF	Lowpass filter	PB. Y
27	MAIN DE-EMPH	Main deemphasis	PB. Y
28	MAIN EMPH	Main emphsis, carrier interleave, white/dark clip	REC. Y
29	TO/DEV ADJ	Carrier frequency and FM modulation adjust	REC. Y
30	S-DET	S-VHS detect	PB. Y
31	FM MOD	Frequency modulator	REC. Y
32	IM HPF	Highpass filter (1 MHz)	REC. Y
33	G EQ	FM signal frequency response adjust (2)	PB. Y
34	DL	SCPB delay	PB. Y
35	P.EQ	FM signal frequency response adjust (1)	PB. Y
36	FM AGC	FM signal sutomatic gain control	PB. Y
37	DET	FM AGC detect	PB. Y
38	7M LPF	Lowpass filter (7 MHz)	REC. Y
39	2M LPF	Lowpass filter (2 MHz)	PB. C
40	BAND GAP	Reference potential	ALL MODE
41	COLOR KILLER	Color signal removal	PB. C
42	N -> P	NTSC-PAL select	PB. C

Table 3-4-1 IC1 operations (1/2)

•IC1 operations (2/2)

No	Block name	Operation	Proscessing signal
43	KILLER DET OUT	Killer output	PB. C
44	B.D	Color burst level down (-6 dB)	PB. C
45	HPF	Highpass filter (100 kHz)	REC. C
46	BPF	Bandpass filter (3.58 MHz)	REC. C,PB. C
47	COMP	Not used	Not used
48	ACC	Color burst level control	REC. C, PB. C
49	HPF fh TRAP	fH used	PB. C
50	HIFI TRAP	HiFi audio signal removal	PB. C
51	MAIN CONV.1	REC: modulator, PB: demodulator	REC. C, PB. C
52	MAIN CONV.2	Demodulator	PB. C
53	1.3M LPF	Lowpass filter (1.3 MHz)	REC. C, PB. C
54	DL 150n	Delay (150 ns)	PB. C
55	1.3M LPF	Lowpass filter (1.3 MHz)	REC. C, PB. C
56	LEVEL DET1	Signal level detect	PB. C
57	LEVEL DET2	Signal level detect	PB. C
58	VCA	Level control amplifier	REC. C, PB. C
59	LPF	Lowpass filter (2 fsc trap)	PB. C
60	PULSE GEN	Pulse generator	REC. C, PB. C
61	ACC DET(BURST)	Carrier level detect	REC. C, PB. C
62	COLOR KILLER ID DE	Color killer ID detect	PB. C
63	APC SW1	APC switch (APC circuit input)	REC. C, PB. C
64	PB APC	Playback automatic phase control	PB. C
65	REC APC	Recording automatic phase control	REC. C
66	X'tal VCO/OSC	Oscillator (3.58 MHz + 629 kHz)	REC. C, PB. C
67	DOWN CONV	Local frequency 629 kHz converter	REC. C, PB. C
68	PB/REC DISCRI	Side lock preventing frequency control	REC. C, PB. C
69	REC AFC	Recording automatic frequency control	REC. C
70	CR DET 2fsc	Automatic adjuster	REC. C, PB. C
71	4 PHASE GEN	4-phase generator	REC. C, PB. C
72	1/2, 2fL VCO	1/2 frequency divider, 2 fL oscillator	REC. C, PB. C
73	MESECAM DET	MESECAM signal detect	
74	C.K	Color signal removal	REC. C
75	B.E	Color burst level up (6 dB)	REC. C
76	SW 30/25	Drum flipflop detect	REC, PB
77	SSB DATA CLK	Logic circuit (from syscon circuit)	Logic signal
78	CCD CNT	External CCD control	PB. Y, PB. C
79	DET	Signal level detect	A.REC, A.PB
80	LINE MUTE	External output signal mute	A.PB
81	REC MUTE	Recording signal mute	A.REC
82	ATT	Attenuator	A.REC
83	50K HPF	Bypass filter (50 kHz)	Not used
84	DET	Signal level detect	Not used

Table 3-4-1 IC1 operations (2/2)

3.4.3 IC1 signal flow in EE mode

Fig. 3-4-2 illustrates the IC1 internal signal flow in the Electric-to-Electric mode.

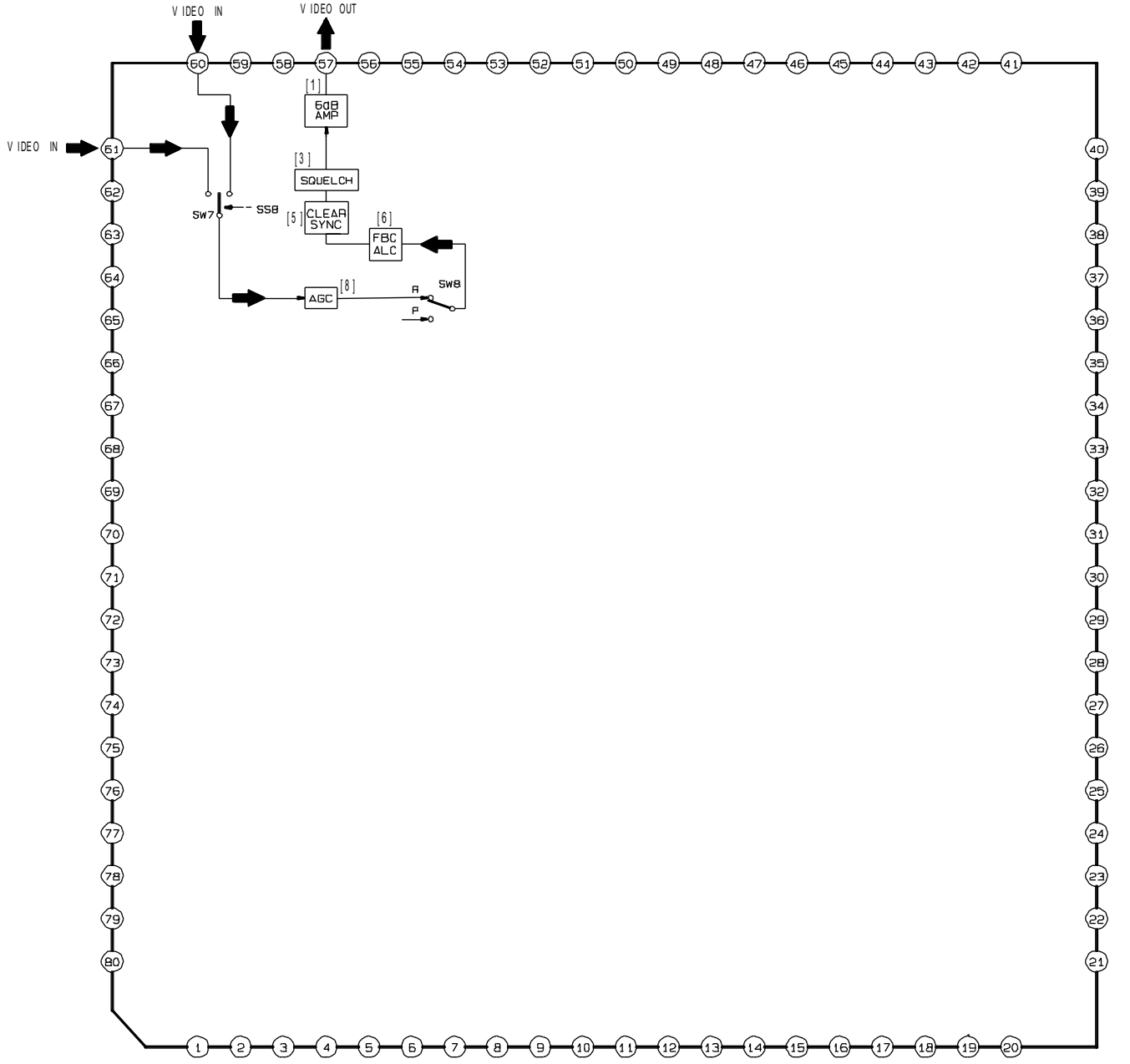


Fig. 3-4-2 EE mode signal flow

3.4.4 IC1 signal flow in REC mode

Fig. 3-4-3 indicates the IC1 internal signal flow in the recording mode.

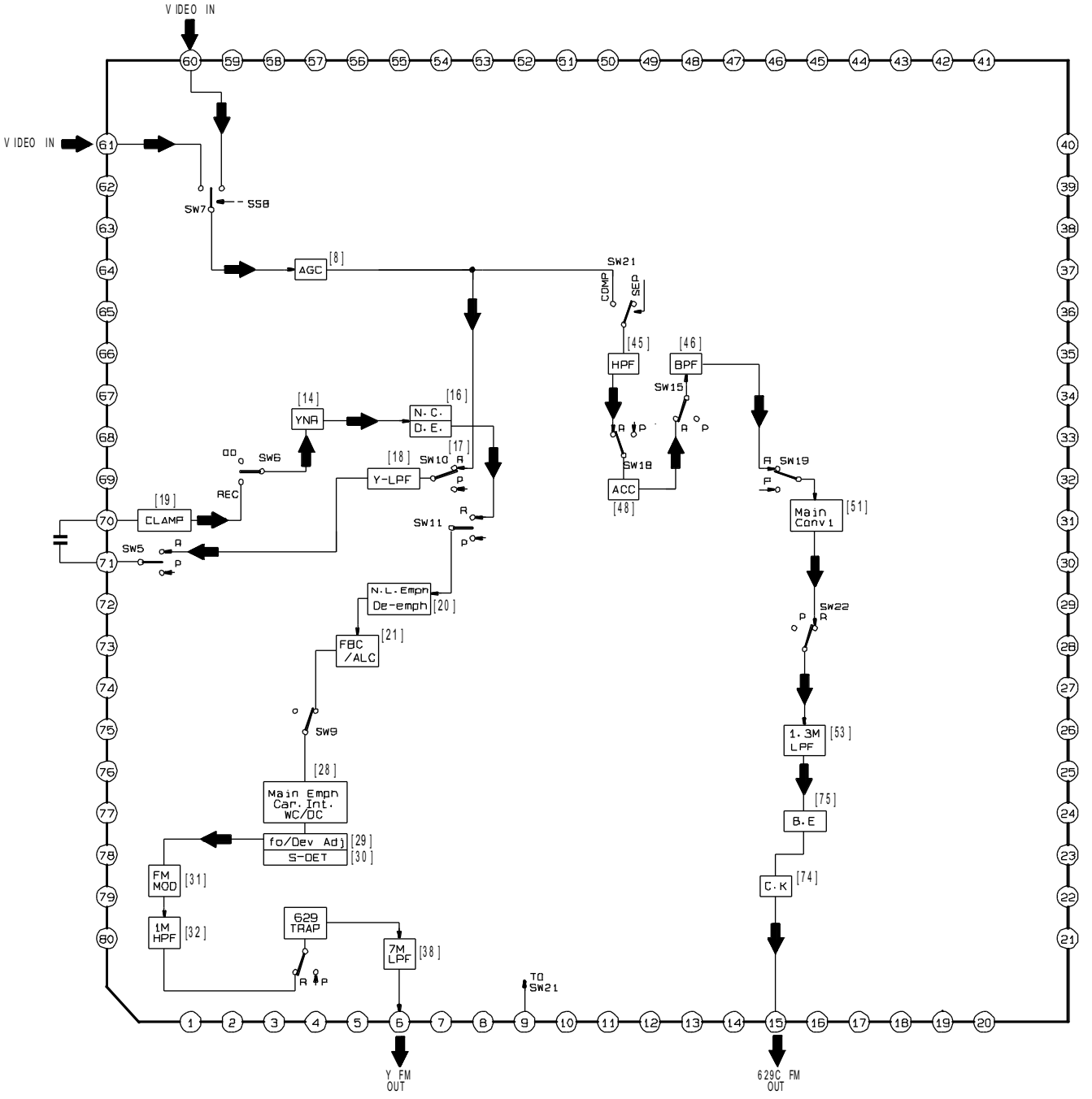


Fig. 3-4-3 REC mode signal flow

3.4.5 IC1 PB mode signal flow

Fig. 3-4-4 shows the IC1 internal signal flow in the playback mode.

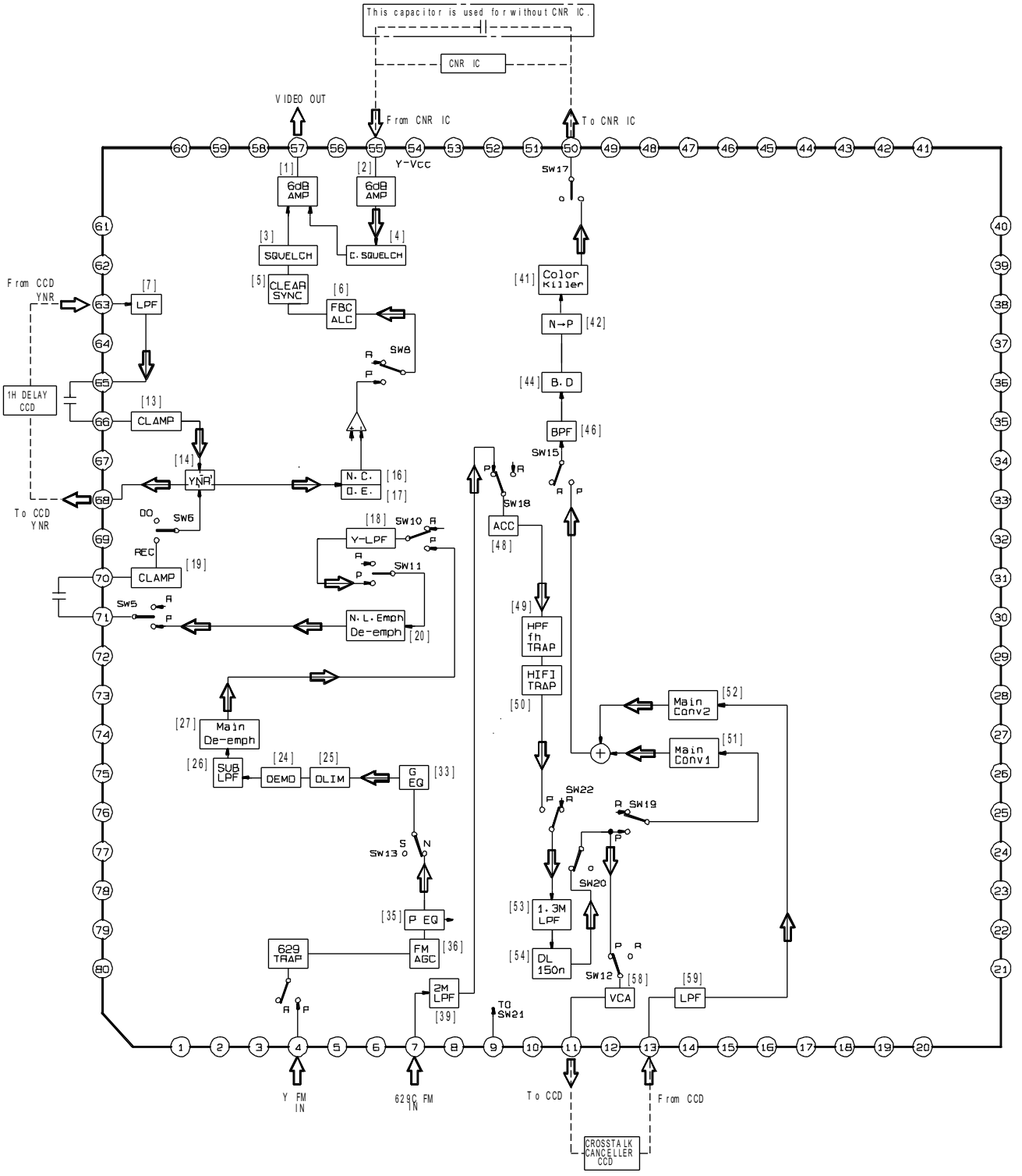


Fig. 3-4-4 PB mode signal flow

SECTION 4
ON-SCREEN CIRCUIT

This section is experience for HR-J231MS as an example.

4.1 ON-SCREEN CIRCUIT

The on-screen circuit is controlled only by IC1301, indicated in Fig. 4-1-1. The circuit functions to superimpose character data on the video signal supplied from the video circuit or on the internally produced blue back signal. When the on-screen functions are not utilized, data indicating absence of characters are superimposed and only the video signal output is visible. The on-screen functions are controlled by the system control (syscon) CPU, which supplies 8 bit serial data to IC1301. The on-screen display is processed by IC1301 on the basis of these control data.

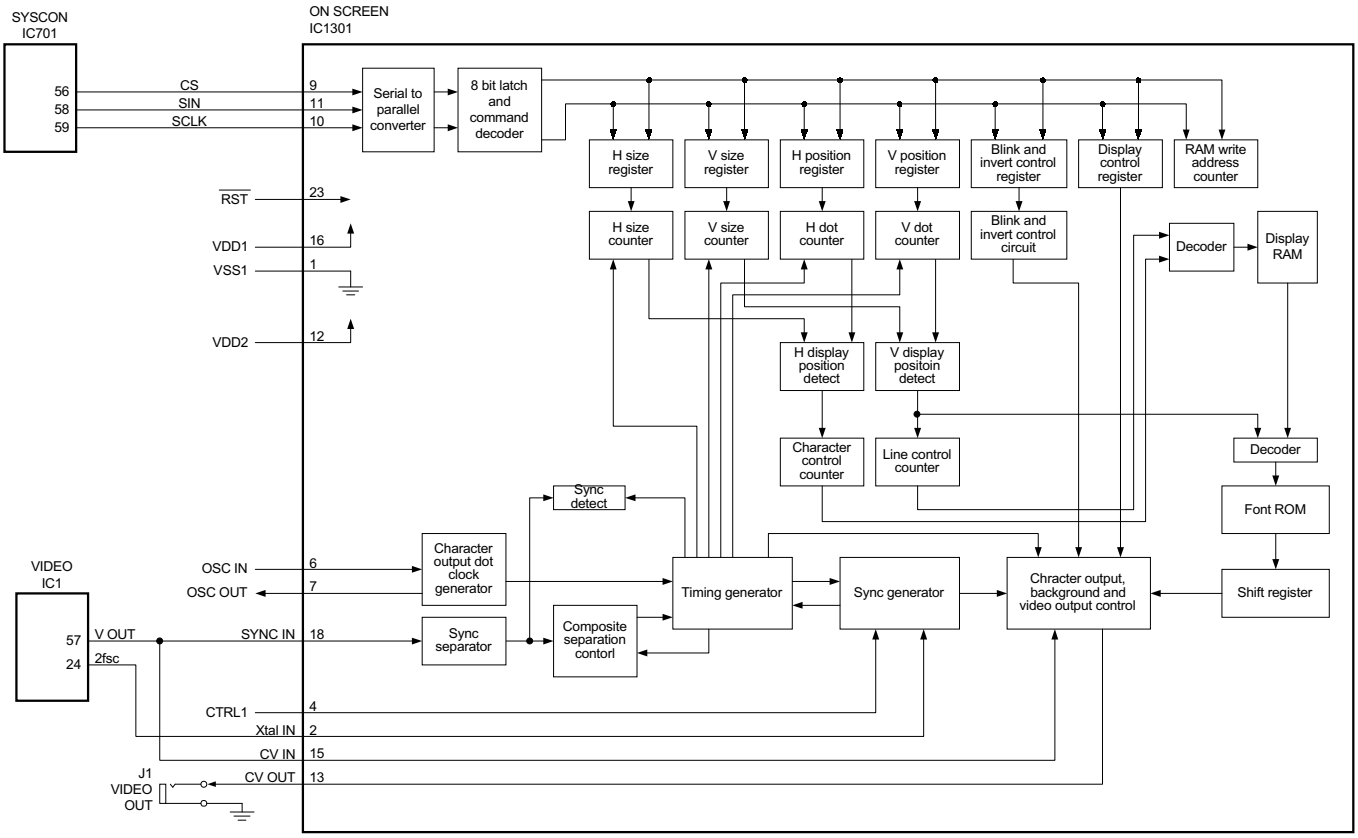


Fig. 4-1-1 On-screen IC block diagram

As indicated in Fig. 4-1-2, the characters are displayed by replacing the video signal with a white signal at the appropriate positions. When the characters are superimposed on the video signal from the video circuit, black borders are provided at the character edges (borders are not produced during blue back). The white character and black border levels are set to lower values than the peak levels.In order to correctly display the characters, external sync is supplied from the video circuit for superimposing the character data on the video signal, and internal sync is generated during blue back. The external sync is separated from the video signal, while the internal sync is produced from the 2fsc signal supplied from the video circuit.

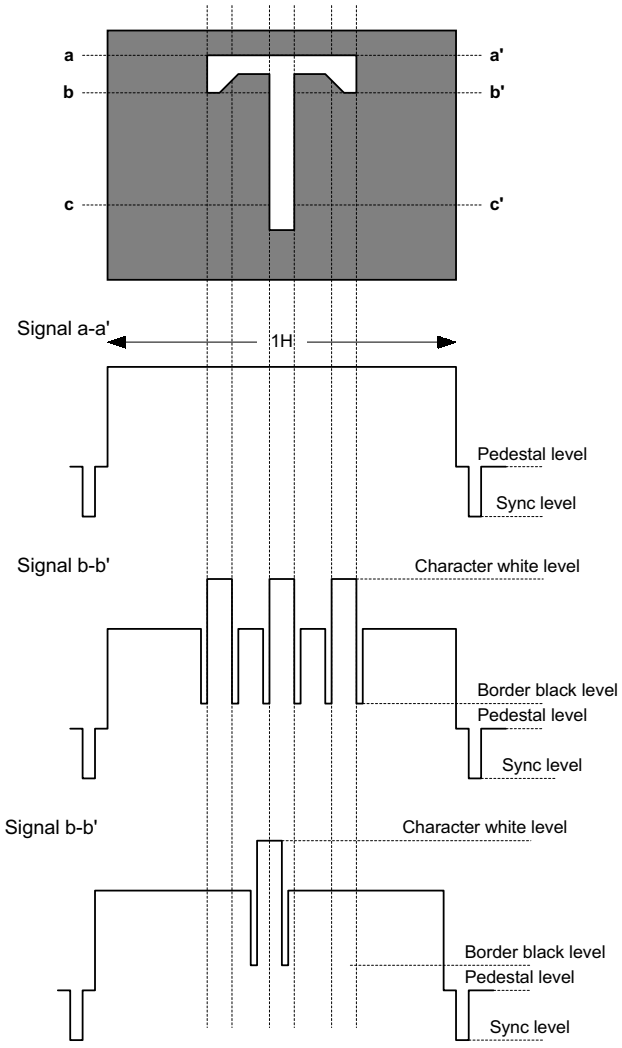


Fig. 4-1-2 Character dispaly signal

4.2 IC1301 FUNCTIONS

Function : VTR on-screen display controller
Screen composition : 24 characters x 12 lines
(max. 288 characters)
Character composition : 12 (H) x 18 (V)
Character types : 128
Display start position : 64 (H) x 64 (V)
Ext. control input : 8 bit serial input
Sync separator : Built-in sync separator circuit

4.2.1 IC1301 pin function

No.	Symbol	Pin name	Function
1	Vss1	Ground	Digital system ground connection
2	XtalIN	Crystal oscillator	External clock (2fsc) input
3	XtalOUT		NC (not connected)
4	CTRL1	Crystal oscillator input select	Select between external clock input and crystal oscillator modes Low: Crystal oscillator, High: External clock input
5	BLANC	Blank output	NC
6	OSCIN	LC oscillator	Coil and capacitor connection for character output dot clock generator
7	OSCOUT		
8	CHARA	Character output	NC
9	CS	Enable input	Low enables serial data input, internal pullup resistance.
10	SCLK	Clock input	Clock for serial data input, internal pullup resistance (hysteresis input).
11	SIN	Data input	Serial data input, internal pullup resistance (hysteresis input).
12	VDD2	Power supply	Power supply (analog system) for adjusting composite video signal level,
13	CVOUT	Video signal output	Composite video signal output.
14	NC		Connected to ground, or not connected.
15	CVIN	Video signal input	Composite video signal input.
16	CVCR	Video signal input	SECAM color signal input.
17	VDD1	Power supply	Digital system power supply, connected to +5 V.
18	STYIN	Sync separator input	Video signal input for internal sync separator circuit.
19	SEPC	Sync separator circuit bias voltage	NC
20	SEPOUT	Composite sync output	NC
21	SEPIN	Vertical sync input	NC
22	CTRL3	SEPIN control	NC
23	RST	Reset input	System reset input, internal pullup resistance (hysteresis input).
24	VDD1	Power supply	Digital system power supply, connected to +5 V.

Table 4-2-1 IC301 pin function

4.2.2 Control data

Control data consists of 8 commands in 8 bit serial form. The first byte is the command identification (ID) code, while the second and subsequent bytes consist of data. The setting commands are as follows.

(1) COMMAND 0 : Display memory (VRAM) write address
(2) COMMAND 1 : Display character data write
(3) COMMAND 2 : Vertical display start position and character size
(4) COMMAND 3 : Horizontal display start position and character size
(5) COMMAND 4 : Display control
(6) COMMAND 5 : Display control
(7) COMMAND 6 : Sync detect
(8) COMMAND 7 : Display control

The on-screen display is controlled by the combination of these commands. The command settings are indicated in Table 4-2-2.

Note: When the 1st byte command ID code is written once, it is stored until the next 1st byte is written. However, if the character display data write command (Command 1) has been entered, the mode is fixed to character display data write and the 1st byte cannot be overwritten. Setting pin CS to High sets the Command 0 (display memory write address setting mode).

Command	1st byte								2nd byte							
	Command ID code				Data				Data							
	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0
COMMAND 0 (write address)	1	0	0	0	V3	V2	V1	V0	0	0	0	H4	H3	H2	H1	H0
COMMAND 1 (character write)	1	0	0	1	0	0	0	at	0	c6	c5	c4	c3	c2	c1	c0
COMMAND 2 (V size and write start position)	1	0	1	0	VS 21	VS 20	VS 11	VS 10	0	FS	VP 5	VP 4	VP 3	VP 2	VP 1	VP 0
COMMAND 3 (H size and write start position)	1	0	1	1	HS 21	HS 20	HS 11	HS 10	0	LC	HP 5	HP 4	HP 3	HP 2	HP 1	HP 0
COMMAND 4 (display control)	1	1	0	0	TST MOD	RAM ERS	OSC STP	SYS RST	0	BLK 2	BLK 1	BLK 0	BK 1	BK 0	RV	DSP ON
COMMAND 5 (display control)	1	1	0	1	NP 1	NP 0	NON	INT	0	0	HLF INT	BCL	CB	PH 2	PH 1	PH 0
COMMAND 6 (sync detect)	1	1	1	0	MOD 1	MOD 0	DIS LIN	MUT	0	RN 2	RN 1	RN 0	SN 3	SN 2	SN 1	SN 0
COMMAND 7 (display control)	1	1	1	1	EX 1	PD 1	EX 0	PD 0	0	CIN SEL	CIN CTL	VNP SEL	VSP SEL	MSK ERS	MSK SEL	EGL

Table 4-2-2 Control data output

1. Command settings

1) Command 0: Display memory (VRAM) write address

• 1st byte
[Command ID code 7 to 4]
Command 0 ID code, display memory write address setting.

[Data 3 to 0 (V3 to V0)]
Display memory line address.

• 2nd byte
[Data 7]
2nd byte ID bit.

[Data 4 to 0 (H4 to H0)]
Display memory column address.

2) Command 1: Display character data write

• 1st byte
[Command ID code 7 to 4]
Command 1 ID code, display character data write setting.

[Data 0 (at)]
Select character attribute off and on.

• 2nd byte
[Data 7]
2nd byte ID bit.

[Data 6 to 0 (c6 to c0)]
Character code.

3) Command 2: Vertical display start position and character vertical size

• 1st byte
[Command ID code 7 to 4]
Command 2 ID code, vertical display start position and character vertical size setting.

[Data 3 and 2 (VS21 and VS20)]
2nd line character V size setting.

[Data 1 and 0 (VS11 and VS10)]
1st line character V size setting.

• 2nd byte
[Data 7]
2nd byte ID bit.

[Data 6 (FS)]
Select crystal oscillator frequency 2 fsc and 4 fsc

[Data 5 to 0 (VP5 to VP0)]
The vertical display start position is designated by 6 bits VP5 - VP0. 1 bit overlap is 2 H.
(VP5: MSB, VP0: LSB)

4) Command 3: Horizontal display start position and character horizontal size

• 1st byte
[Command ID code 7 to 4]
Command 3 ID code, horizontal display start position and character horizontal size setting.

[Data 3 and 2 (HS21 and HS20)]
2nd line character H size

[Data 1 and 0 (HS11 and HS10)]
1st line character H size

• 2nd byte
[Command ID code 7]
2nd byte ID bit

[Command ID code 6]
Use LC oscillator or crystal oscillator for dot clock.
Select dot clock used for character horizontal display direction.

[Command ID code 5 (HP5 to HP0)]
The horizontal display start position is designated by 6 bits HP5 - HP0. 1 bit overlap is 2 Tc.
(HP5: MSB, HP0: LSB)

5) Command 4: Display control setting

• 1st byte
[Command ID code 7 to 4]
Command 4 ID code, display control setting.

[Data 3 (TSTMOD)]
Normal operation or test mode select (Fix at 0: normal operation).

[Data 2 (RAMERS)]
Display RAM erase (set to 7F HEX).

[Data 1 (OSCSTP)]
Do not stop crystal and LC oscillator circuits or stop crystal and LC oscillator circuits.

[Data 0 (SYSRST)]
Reset all registers, display off.

• 2nd byte
[Data 7]
2nd byte ID bit.

[Data 6 (BLK2)]
Character display area or video display area select.
Designate overall superimpose size.

[Data 5 and 4 (BLK1 and 0)]
Blanking size variation.

[Data 3 (BK1)]
Blanking period select.

[Data 2 (BK0)]
Select character blink off and on.
Negative character blinking is between positive and negative characters.

[Data 1 (RV)]
Select reverse (negative characters) off and on.

[Data 0 (DSPON)]
Select character display off and on.

6) Command 5: Display control setting

• 1st byte
[Command ID code 7 to 4]
Command 5 ID code, display control setting.

[Data 3 and 2 (NP1 and NP0)]
Select among NTSC, PAL, PAL-M and PAL-N.

[Data 1 (NON)]
Select between interlace and non-interlace.

[Data 0 (INT)]
Select between external and internal sync.

• 2nd byte
[Data 7]
2nd byte ID bit.

[Data 5 (HLFINT)
Select between normal mode and semi-internal sync mode.

[Data 4 (BCL)]
Select between background color present and absent (only background level set).

[Data 3 (CB)]
Select between color burst signal output present and stopped.

[Data 2 to 0 (PH2 to PH0)]
Select background color phase with respect to burst.

7) Command 6: Sync signal detect

• 1st byte

[Command ID code 7 to 4]
Command 6 ID code, sync signal control setting.

[Data 3 (MOD1)]
Select between sync separation signal and high output during internal sync.

[Data 2 (MOD0)]
Select Blank (pin 5) and Character (pin 8) outputs.

[Data 1 (DISLIN)]
Select display line 12 and 10.

[Data 0 (MUT)]
Select normal output and cut CVIN and fix CVOUT to pedestal level.

• 2nd byte

[Data 7]
2nd byte ID bit.

[Data 6 to 4 (RN2 toRN0)]
Detects presence or absence of signal controlling external sync signal detection. Sets sampling interval for enabling continuous sync detection in the horizontal sync period (1 H).

[Data 3 to 0 (SN3 to SN0)]
Detects presence or absence of signal controlling external sync signal detection. Sets sampling interval for enabling continuous sync detection in the horizontal sync period (1 H).

8) Command 7: Display control setting

• 1st byte

[Command 7 to 4]
Command 7 ID code, display control setting.

[Data 3 (EX1)]
Select MODE 1 setting and PORT DATA 1 setting for SEPOUT (pin 19) output.

[Data 2 (PD1)]
Select output Low setting and High setting.

[Data 1 (EX0)]
Select MODE 0 setting and PORT DATA 0 setting for BLANK (pin 5) output.

[Data 0 (PD0)]
Select output Low setting and High setting.

• 2nd byte

[Data 7]
2nd byte ID bit.

[Data 6 (CINSEL)]
Select Blank (character and border OR signal) area and Video signal area for CVCR On signal.

[Data 5 (CINCTL)]
CVCR on/off.

[Data 4 (VNPSEL)]
Selects V polarity for external mode and internal V separation.

[Data 3 (VSPSEL)]
Internal V separation time select.

[Data 2 (MSKERS)]
Select Mask enable and disable for H and V sync mask release.

[Data 1 (MSKSEL)]
V sync mask select.

[Data 0 (EGL)]
Border level select.

4.2.3 Display screen composition

The display screen is composed of 24 characters by 12 lines.
The maximum character display is 288.
When the character size is enlarged, the maximum character display is less than 288.
The display memory address is designated by line address (0DEC - 11DEC) and column address (0DEC - 23DEC).

Display screen composition (display memory addresses)

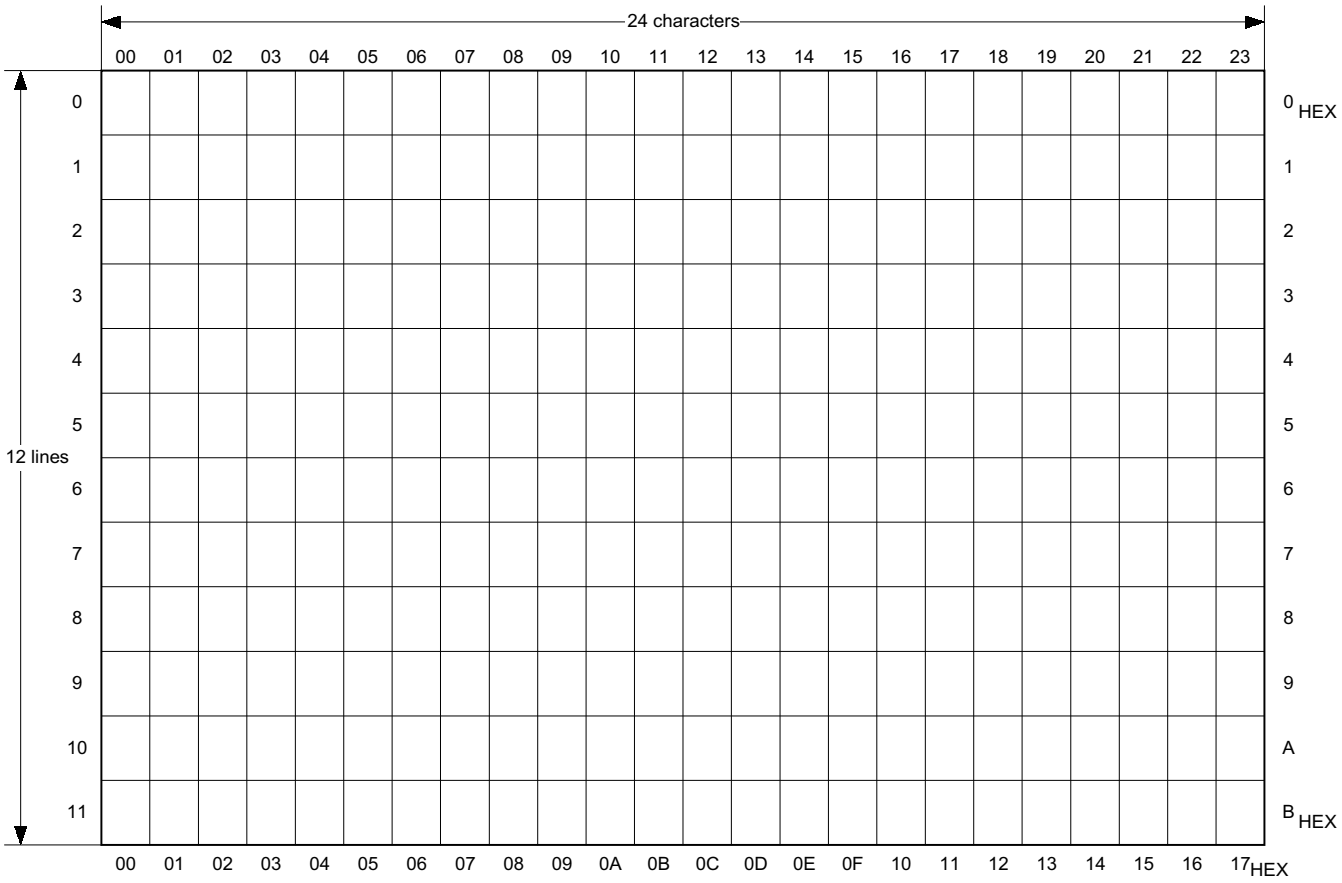


Fig. 4-2-1 Display screen composition

4.3 CHARACTER DISPLAY EXAMPLE

By using the commands, characters can be displayed on the character display area as indicated in the Fig. 4-3-1 example.

1) Commands 2 and 3 determine the character size of the 1st and 2nd lines and character display area start position on TV display.

* Only the character size of the 1st and 2nd lines can be designated.
* Commands 2 and 3 respectively determine the vertical and horizontal directions.

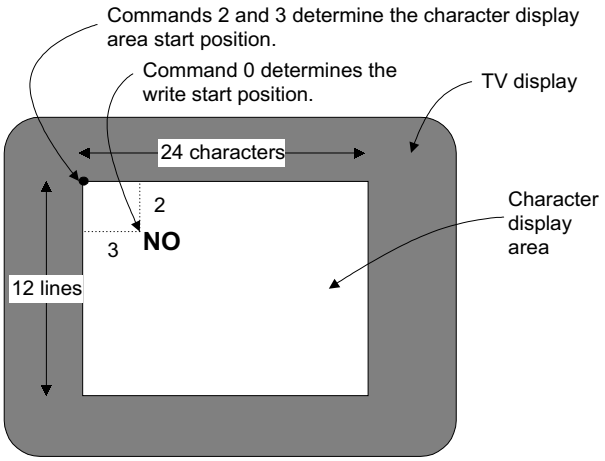


Fig. 4-3-1 Character display area

2) Command 0 determines the write start position in character display area.

In this example, vertical position 2 and horizontal position 3 are expressed in binary form.

2: 0010
3: 0011

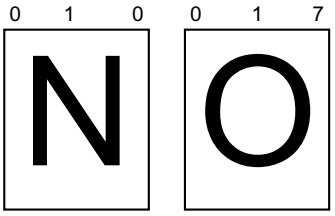
The command data are then: 1000, 0010, 0000 and 0011.

3) Command 1 selects the character type.

* 128 types of characters can be stored. A blank space is also stored as 1 character.
* Each character is provided with a base 16 number.
* When a base 16 number is sent as data, 7 bits are required for 128 types.

* Example

By using the character number in the Fig. 4-3-2.



In this case:
010 : 0001, 0000
017 : 0001, 0111
Command 1 is:
1001, 0000, 0001, 0000
1001, 0000, 0001, 0111

Fig. 4-3-2 Example of character number vs command 1 data

SECTION 5
POWER SUPPLY CIRCUIT AND TROUBLESHOOTING

This section is experience for HR-VP830U as an example.

5.1 BASIC OPERATION

Refer to Fig. 5-1-1 the switching regulator schematic diagram.

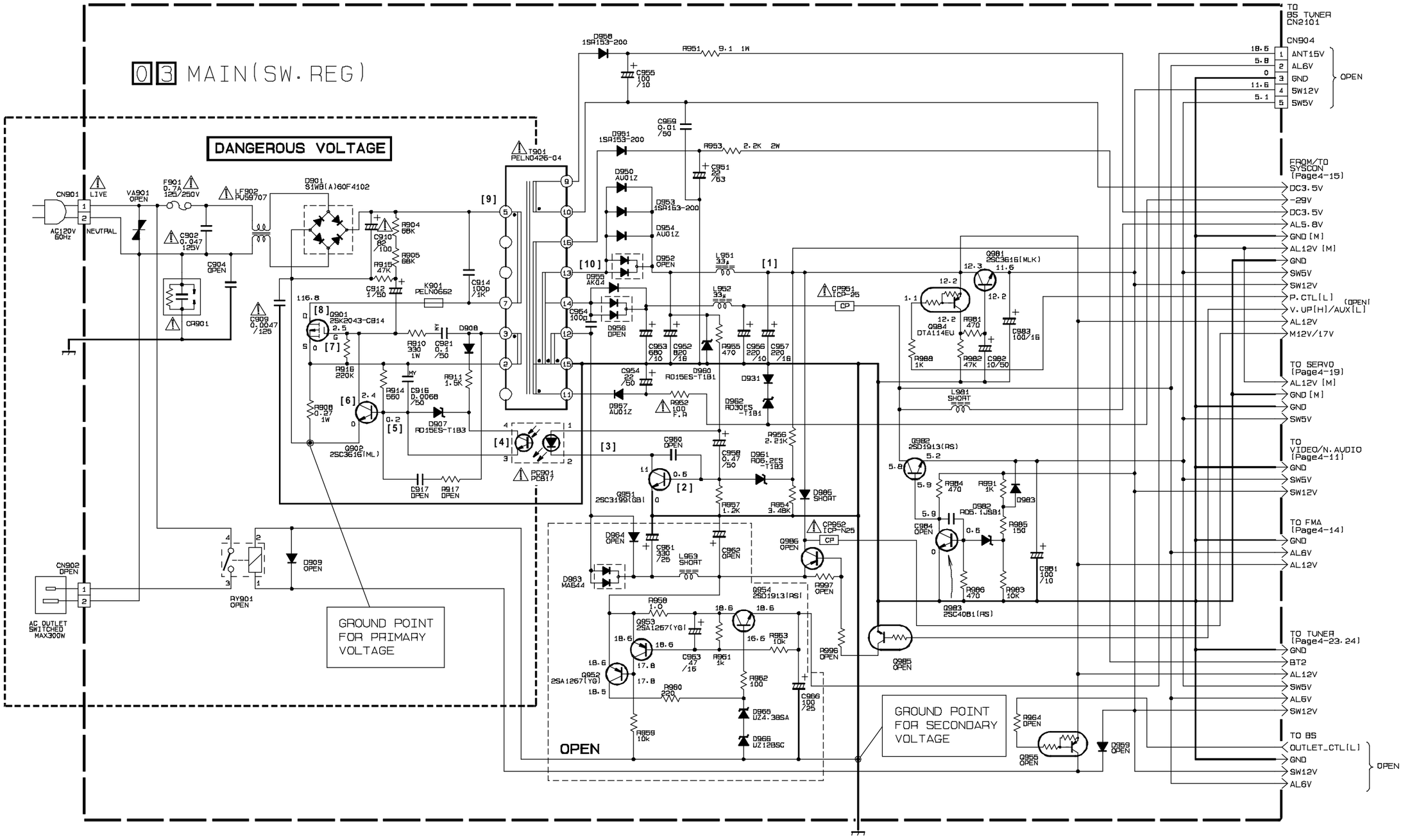


Fig. 5-1-1 Switching regulator schematic diagram

The circuit system is termed a ringing choke coil (RCC) switching regulator.
In this system, feedback from the secondary output voltage fluctuations controls the primary oscillation frequency. The energy transferred to the secondary is varied to thereby stabilize the secondary output voltage.
Feedback in the present circuit is from the secondary AL12V voltage variations to the primary. Since the AL12V output voltage load is greatest, by stabilizing this voltage, the other output voltages are effectively stabilized. In this manner, the RCC type switching regulator continuously returns variations of the output voltage having maximum load to the primary.
The Fig. 5-1-2 flowchart illustrates the process for applying feedback from AL12V output voltage fluctuations.

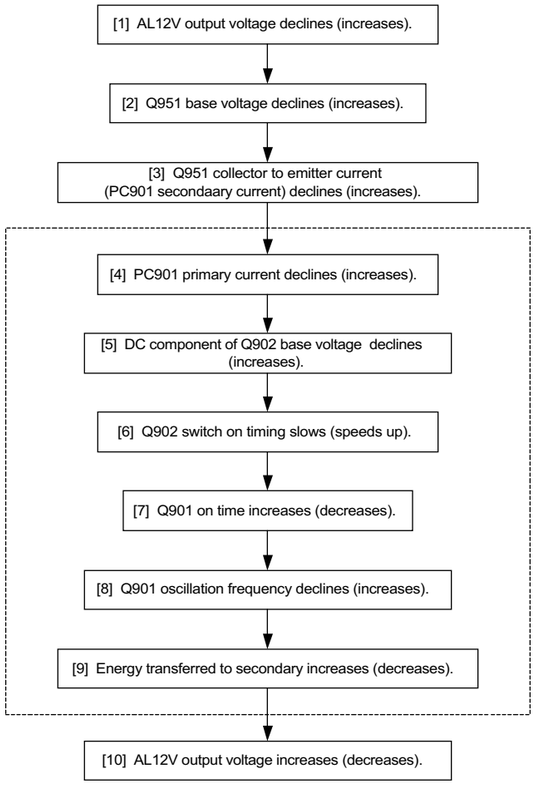


Fig. 5-1-2 Power supply feedback loop operation

Oscillation frequency control in the primary (outlined area of Fig. 5-1-2) is indicated in Fig. 5-1-3. The process from supply of AC power to the end of the first oscillation cycle is described.

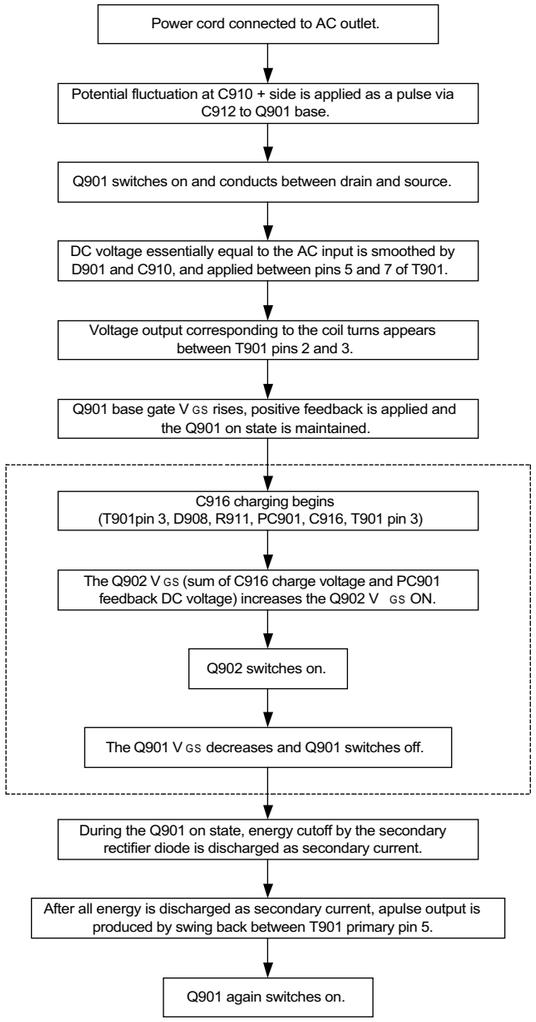
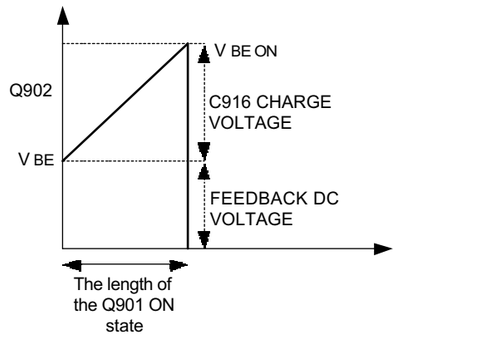


Fig. 5-1-3 Oscillator circuit operation

The length of the Q901 on state (timing for switching Q901 off) is determined by operations indicated by the dotted outline in Fig. 5-1-3. The on state duration is thus determined by DC voltage feedback as current from PC901 and C916 charge voltage (refer to Fig. 5-11-4).



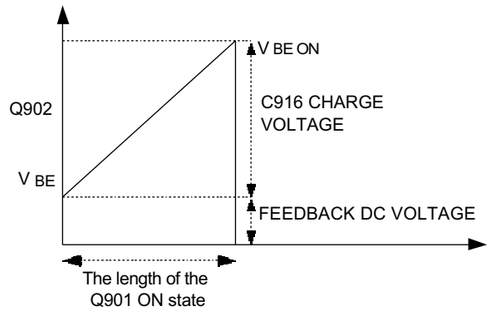


Fig. 5-1-4 The length of the Q901 on state

The oscillator circuit parts characteristics determine the C916 charge voltage risetime, while the feedback current from PC901 varies according to the secondary load, as indicated in Fig. 5-1-2. Consequently, the secondary load determines the Q901 on period as follows.
a) Secondary load increase: Q901 on state duration increases (T901 stored energy maximum).
b) Secondary load decrease: Q901 on state duration decreases (T901 stored energy minimum).
During the Q901 on state, the energy stored in T901 is discharged to the secondary and does not appreciably control the Q901 off state duration. However, this is essentially the same as the on state: longer with increased load and shorter with decreased load.
Therefore, the time of one Q901 oscillation cycle (total on and off state duration) is determined by the secondary load. In other words, the secondary load determines the Q901 oscillation frequency.

5.2 POWER SUPPLY CIRCUIT PROTECTION

5.2.1 Secondary overload protection

C912 charges during the Q901 off state. When the secondary load exceeds a predetermined value, C912 becomes fully charged during the Q901 off state. The pulse input to Q901 gate through C912 ceases and circuit oscillation stops without entering the next cycle.
In order to restore circuit operation in this event, disconnect the power cord from the AC outlet and wait a sufficient time for C912 to discharge.

5.2.2 Secondary overvoltage protection

In event of abnormal increase in the secondary output voltage to where the AL12V output voltage exceeds a predetermined value, D960 shorts and the load sharply increases. This activates the overload protection system described above and oscillation stops.

5.2.3 Primary overcurrent protection

In event Q901 IDS increases and Q901 source voltage increases beyond a predetermined value, Q902 switches on and Q901 switches off and oscillation stops. In this case, circuit operation is restored when the IDS declines below the excess value.

5.3 POWER SUPPLY TROUBLESHOOTING

The following types of failures can occur in this circuit.

5.3.1 Power not supplied (Q901 oscillation waveform completely absent)

In this case, inspect the following components.

(1) Q901 shorted or open.
(2) Q902 shorted.
(3) F901 open.
(4) Defective excitation circuit components, e.g., R904, R905, C912, etc.

5.3.2 Power not supplied (Q901 oscillation waveform occurs briefly, but stops immediately)

Inspect for the following types of failures.

(1) Q901 and Q902 shorted or open (be sure to replace both simultaneously).
(2) Defective components in the switching regulator feedback loop causing abnormal rise in secondary output voltage. The secondary overvoltage protector system operates and D960 shorts.
(3) Defective components in the switching regulator feedback loop causing abnormal IDS current. The primary over-current protector system operates.
(4) Short between the secondary or load circuit and ground. The secondary overload protector system operates.

JVC

VICTOR COMPANY OF JAPAN, LIMITED

Printed in U.S.A.
9704 (YTC-EY)