JVC

VIDEO TECHNICAL GUIDE

VIDEO CASSETTE RECORDER

HR-S9500 NTSC/PAL/SECAM

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SECTION 1
VIDEO CIRCUIT

1.1 CIRCUIT CONFIGURATION IN GENERAL

Let us discuss signal processing in general taking the HR-S9500U as an example.
As can be seen from the video block diagram of the Service Manual, the video circuitry consists of the VIDEO/ONSCREEN (MAIN board) circuit and the VIDEO, 3D/TBC (3D SVHS board) circuit.
The VIDEO, 3D/TBC (3D SVHS board) consists mainly of the IC1 which carries out normal video signal processing. This IC has been made by combining together the video signal processor IC and the pre-recorder IC used in the 1997 model . It therefore basically takes over the functions of those two ICs, except for a newly introduced function for the SVHS ET system.
The VIDEO, 3D/TBC (3D SVHS board) circuit consists of a SVHS system's proper circuit made up of an IC1001 and an IC1002 and a picture quality enhancer which consists mainly of an IC1401 (IC1201 in some models).
In the 1998 version, while all the models are equipped with the VIDEO/ON SCREEN (MAIN board) circuit, the VIDEO, 3D/TBC (3D SVHS board) circuit is included only in the SVHS models.
All this is summarized in Table 1-1-1.

1.1.1 Table of video types (1/4)

	MODEL	MAIN PWB	3D SVHS or 2D SVHS PWB		TRI-R PWB
			SVHS	Y/C SEPA AND NR	IC501
		IC1 (VIDEO PROCESS)	IC1001 (JCP8008) and IC1002 (VC2076MP)	3D (IC1401:JCP8010) or 2D (IC1201:JCP8013)	or IC3001 (JCP0065)
U	HR-A34U	HA118211BNF	Not used		Not used
	HR-A54U	HA118211BNF	Not used		Not used
	HR-VP450U	HA118211BNF	Not used		Not used
	HR-VP453U	HA118211BNF	Not used		Not used
	HR-VP452U	HA118211BNF	Not used		Not used
	HR-VP650U	HA118211BNF	Not used		Not used
	HR-VP653U	HA118211BNF	Not used		Not used
	HR-VP652U	HA118211BNF	Not used		Not used
	HR-VP654U	HA118211BNF	Not used		Not used
	HR-VP655U	HA118211BNF	Not used		Not used
	HR-VP656U	HA118211BNF	Not used		Not used
	HR-DD750U	JCP8016-NSA/NSB/NVA/NVB	Not used		Not used
	HR-VP658U	HA118211BNF	Not used		IC501
	HR-S3500U	JCP8016-NSB	Used	2D	Not used
	HR-S4500U	JCP8016-NSB	Used	2D	Not used
	HR-S7500U	JCP8016-NSB	Used	3D	Not used
	HR-S9500U	JCP8016-NSB	Used	3D	Not used

Table 1-1-1 Table of video types (1/4)

· Table of video types (2/4)

	MODEL	MAIN PWB	3D SVHS or 2D SVHS PWB		TRI-R PWB
			SVHS	Y/C SEPA AND NR	IC501
		IC1 (VIDEO PROCESS)	IC1001 (JCP8008) and IC1002 (VC2076MP)	3D (IC1401:JCP8010) or 2D (IC1201:JCP8013)	or IC3001 (JCP0065)
U(C)	HR-A34U(C)	HA118211BNF	Not used		Not used
	HR-A54U(C)	HA118211BNF	Not used		Not used
	HR-VP453U(C)	HA118211BNF	Not used		Not used
	HR-VP650U(C)	HA118211BNF	Not used		Not used
	HR-VP653U(C)	HA118211BNF	Not used		Not used
	HR-VP654U(C)	HA118211BNF	Not used		Not used
	HR-VP656U(C)	HA118211BNF	Not used		Not used
	HR-DD750U(C)	JCP8016-NSA/NSB/NVA/NVB	Not used		Not used
	HR-VP658U(C)	HA118211BNF	Not used		IC501
	HR-S3500U(C)	JCP8016-NSB	Used	2D	Not used
	HR-S7500U(C)	JCP8016-NSB	Used	3D	Not used
UM	HR-J4005UM	HA118211BNF	Not used		Not used
	HR-J3005UM	HA118211BNF	Not used		Not used
	HR-J4405UM	HA118211BNF	Not used		Not used
	HR-J6005UM	HA118211BNF	Not used		Not used
	HR-J7005UM	HA118211BNF	Not used		Not used
T	HR-DD2000T	JCP8016-NSA/NSB/NVA/NVB	Not used		Not used
	HR-DD2100T	JCP8016-NSB	Used	2D	Not used
E	HR-J250E	HA118211F/AF/BF	Not used		Not used
	HR-J258E	HA118211F/AF/BF	Not used		Not used
	HR-J458E	HA118211F/AF/BF	Not used		Not used
	HR-J658E	JCP8016-MSA/MSB	Not used		Not used
	HR-J700E	JCP8016-MSA/MSB	Not used		Not used
	HR-J758E	JCP8016-MSA/MSB	Not used		IC3001
	HR-DD858E	JCP8016-MSA/MSB	Not used		IC3001
	HR-S7500E	JCP8016-MSB	Used	2D	Not used
	HR-S8500E	JCP8016-MSB	Used	3D	Not used
	HR-S9500E	JCP8016-MSB	Used	3D	Not used
EK	HR-J255EK	HA118211AF/BF	Not used		Not used
	HR-J256EK	HA118211AF/BF	Not used		Not used
	HR-J455EK	HA118211F/AF/BF	Not used		Not used
	HR-J655EK	JCP8016-MSA/MSB	Not used		Not used
	HR-J755EK	JCP8016-MSA/MSB	Not used		IC3001
	HR-DD855EK	JCP8016-MSA/MSB	Not used		IC3001
	HR-S7500EK	JCP8016-MSB	Used	2D	Not used
	HR-S9500EK	JCP8016-MSB	Used	3D	Not used

Table 1-1-1 Table of video types (2/4)

· Table of video types (3/4)

	MODEL	MAIN PWB	3D SVHS or 2D SVHS PWB		TRI-R PWB
			SVHS	Y/C SEPA AND NR	IC501
		IC1	IC1001 (JCP8008)	3D (IC1401:JCP8010)	or
		(VIDEO PROCESS)	and	or	IC3001
			IC1002 (VC2076MP)	2D (IC1201:JCP8013)	(JCP0065)
EH	HR-J658EH	JCP8016-MSA/MSB	Not used		Not used
	HR-J758EH	JCP8016-MSA/MSB	Not used		IC3001
	HR-DD858EH	JCP8016-MSA/MSB	Not used		IC3001
	HR-S7500EH	JCP8016-MSB	Used	2D	Not used
	HR-S8500EH	JCP8016-MSB	Used	3D	Not used
	HR-S9500EH	JCP8016-MSB	Used	3D	Not used
EA	HR-J255EA	HA118211AF/BF	Not used		Not used
	HR-J455EA	HA118211AF/BF	Not used		Not used
	HR-J655EA	JCP8016-MSA/MSB	Not used		Not used
	HR-S5500AMEA	JCP8016-MSB	Used	2D	Not used
EN	HR-J452EN	HA118211BLF	Not used		Not used
	HR-J456EN	HA118211BLF	Not used		Not used
	HR-J656EN	HA118211BLF	Not used		Not used
ES	HR-J255ES	HA118211AF/BF	Not used		Not used
M	HR-J454M	HA118211BLF	Not used		Not used
	HR-J453M	HA118211BLF	Not used		Not used
	HR-J653M	HA118211BLF	Not used		Not used
	HR-J656M	HA118211BLF	Not used		Not used
	HR-DD750M	JCP8016-LSA/LSB	Not used		Not used
ED	HR-P23KD	HA118211BF	Not used		Not used
	HR-P331KD	HA118211BF	Not used		Not used
EE	HR-P135EE	HA118211BF	Not used		Not used
	HR-P138EE	HA118211BF	Not used		Not used
	HR-J258EE	HA118211F/AF/BF	Not used		Not used
	HR-J255EE	HA118211F/AF/BF	Not used		Not used
	HR-J259EE	HA118211F/AF/BF	Not used		Not used
	HR-J458EE	HA118211AF/BF	Not used		Not used
	HR-J459EE	HA118211AF/BF	Not used		Not used
	HR-J658EE	JCP8016-MSA/MSB	Not used		Not used
	HR-J759EE	JCP8016-MSA/MSB	Not used		IC3001
	HR-S7500EE	JCP8016-MSB	Used	2D	Not used
EM	HR-J351EM	HA118211AF/BF	Not used		Not used
	HR-J457MS	HA118211AF/BF	Not used		Not used

Table 1-1-1 Table of video types (3/4)

· Table of video types (3/4)

	MODEL	MAIN PWB	3D SVHS or 2D SVHS PWB		TRI-R PWB
			SVHS	Y/C SEPA AND NR	IC501
		IC1	IC1001 (JCP8008)	3D (IC1401:JCP8010)	or
		(VIDEO PROCESS)	and	or	IC3001
			IC1002 (VC2076MP)	2D (IC1201:JCP8013)	(JCP0065)
A	HR-J251MS	HA118211AF/BF	Not used		Not used
	HR-J457MS/A	HA118211AF/BF	Not used		Not used
	HR-J657MS	JCP8016-MSA/MSB	Not used		Not used
	HR-J657MS/S	JCP8016-MSA/MSB	Not used		Not used
	HR-DD857MS	JCP8016-MSA/MSB	Not used		IC3001
	HR-S5500AM	JCP8016-MSB	Used	2D	Not used
	HR-JP12A	HA118211BF	Not used		Not used
	HR-P42A	HA118211BF	Not used		Not used
	HR-P52A	HA118211BF	Not used		Not used
	HR-P72K	HA118211BF	Not used		Not used
	HR-JP32K	HA118211BF	Not used		Not used
	HR-P92K	HA118211AF/BF	Not used		Not used
	HR-P92K/S	HA118211AF/BF	Not used		Not used
MS	HR-J256MS	HA118211F/BF	Not used		Not used
	HR-J456MS	HA118211F/BF	Not used		Not used
	HR-J656MS	JCP8016-MSA/MSB	Not used		Not used
	HR-J656MS(C)	JCP8016-MSA/MSB	Not used		Not used
	HR-DD659MS	JCP8016-MSA/MSB	Not used		Not used
	HR-J756MS	JCP8016-MSA/MSB	Not used		Not used
	HR-DD859MS	JCP8016-MSA/MSB	Not used		Not used
	HR-S7500MS	JCP8016-MSB	Used	2D	Not used
	HR-S8500MS	JCP8016-MSB	Used	3D	Not used
	HR-S9500MS	JCP8016-MSB	Used	3D	Not used
SA	HR-J255SA	HA118211AF/BF	Not used		Not used

Table 1-1-1 Table of video types (3/4)

1.2 SIGNAL PROCESSING IN GENERAL

Let us discuss signal processing in general taking the HR-S9500U as an example.

1.2.1 Signal processing during recording

Fig. 1-2-1 shows a video signal flow chart during recording.

1) Y-signal processing

The composite input signals from the front and rear tuners are fed to pins 50, 18 and 52 of IC1001. Those input signals are selected by SW24. The composite input signals then undergo AGC and FBC processing and are separated between Y and C components at IC1401. The Y signal is then delivered to IC1001.

On the other hand, the S input Y signals from the front and rear tuners are selected at IC1003 and fed to pin 46 of IC1001 in order to undergo AGC and other processing.

Selection between the composite input mode and the S input mode is accomplished by SW1 and SW6.

The Y signal, after passing through the N/S-LPS, undergoes non-linear emphasis processing at IC1002

in the SVHS mode, and is then delivered to IC1 as it is in the VHS mode.
The signal is subjected to normal FM modulation processing at IC1.

2) C-signal processing

The C component of the composite input signal is likewise separated from the Y component at IC1401 and is delivered to IC1001.
Selection of the S input C signal between the front and rear tuners is accomplished by IC1003.
The C signal is then delivered to IC1 via IC2 (REC/PB selector) and undergoes normal low-frequency range conversion processing.

1.2.2 Signal processing during playback

Fig. 1-2-2 shows a video signal flow chart during playback.

1) Y signal processing

The FM signal from the video head is fed to the pre-amp section of IC1 and is then delivered from pin 79.
Upon switching IC2, the signal passes through the equalizer in the SVHS mode, while going to IC1 as it is, for normal FM demodulation processing in the VHS mode.
The Y signal after FM demodulation is sent to IC1001 and is subjected to non-linear de-emphasis processing at IC1002 in the SVHS mode, while going directly to IC1001 in the VHS mode.
The Y signal is then sent to IC1 again and undergoes YNR, DE, APT and ALC processing to go out of IC1.
It is finally subjected to NR processing (see Sec. 2 for details) at IC1401 and is again delivered to IC1001. Thereafter, the S output signal goes through pin 26 to be delivered from the S output connector of the rear tuner.
The composite output is sent to the adder section to be added to the C signal.
After addition, the composite signal going through pin 23 is subjected to onscreen processing at IC201 and is then sent to the composite output terminal and the RF converter of the rear tuner.
Note that for the S output of the onscreen menu, the composite signal delivered from IC201 is fed to pin 25 of IC1001 and is then internally separated between Y and C to be output like a normal Y signal.

2) C signal processing

The FM signal from the video head is delivered to the pre-amp section of IC1. The C component is then taken out of it at 2MLPF and CLPF and is subjected to normal C signal demodulation processing.
Note that this IC demodulator employs the double main converter system introduced with the 1996 models. See the Technical Guide (VTG82081) of the HR-VF830U/E939EG/J936MS for details.
The demodulated C signal undergoes B.D and other processing to be delivered from IC1.
The C signal is then subjected to NR processing (see Sec. 2 for details) at IC1401 and is fed to IC1001.
The S output signal goes through pin 21 and is delivered from the S output terminal of the rear tuner.
The composite output is sent to the adder with the Y signal to be processed as described for the Y signal.
The S output signal for the onscreen menu is processed as described for the Y signal.

1.2.3 Signal processing during EE

The video signal flow for the EE system is shown in Fig. 1-2-3 for reference.

· Signal processing during recording (1/4)

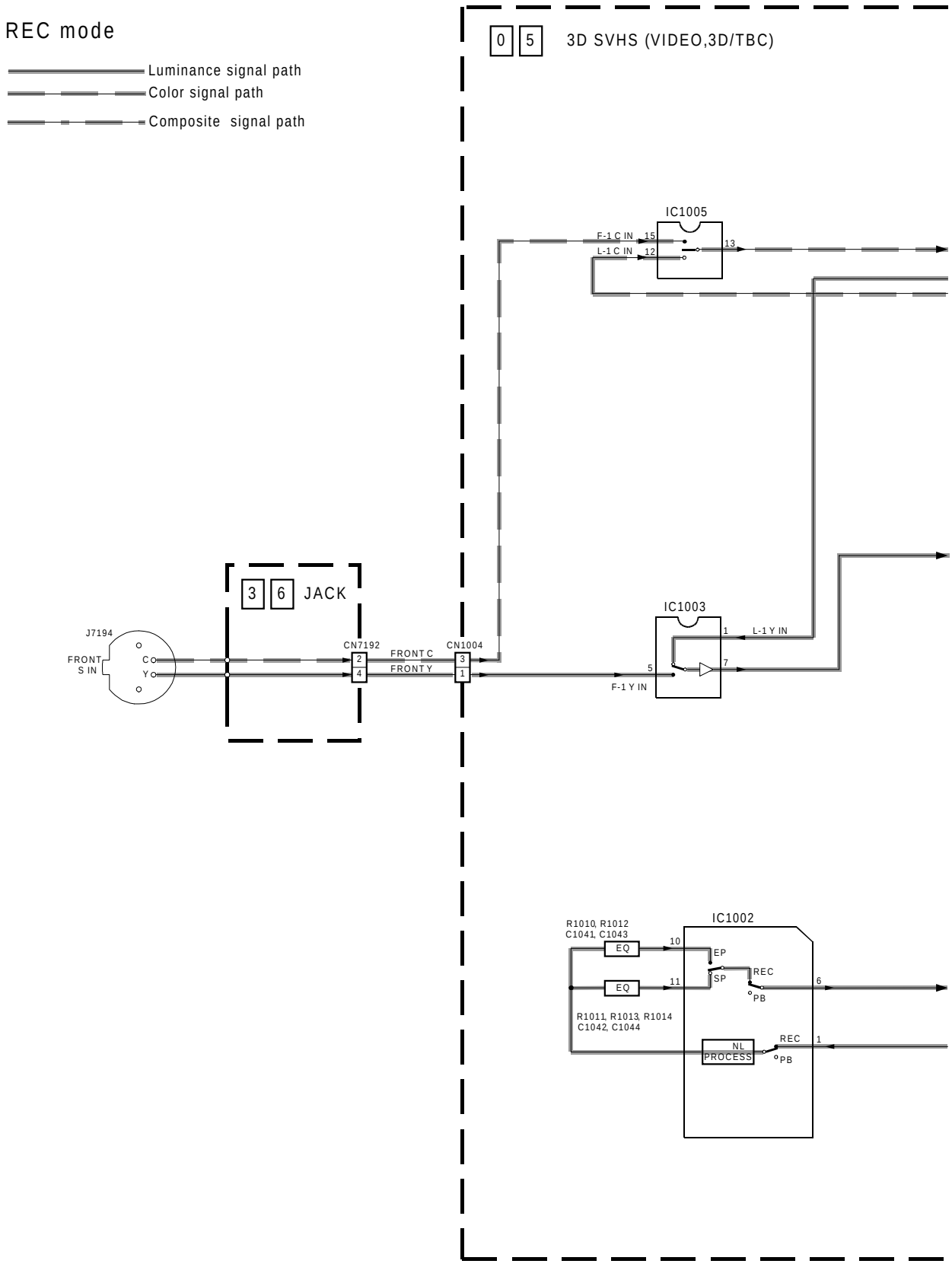

Fig. 1-2-1 Signal processing during recording (1/4)

· Signal processing during recording (2/4)

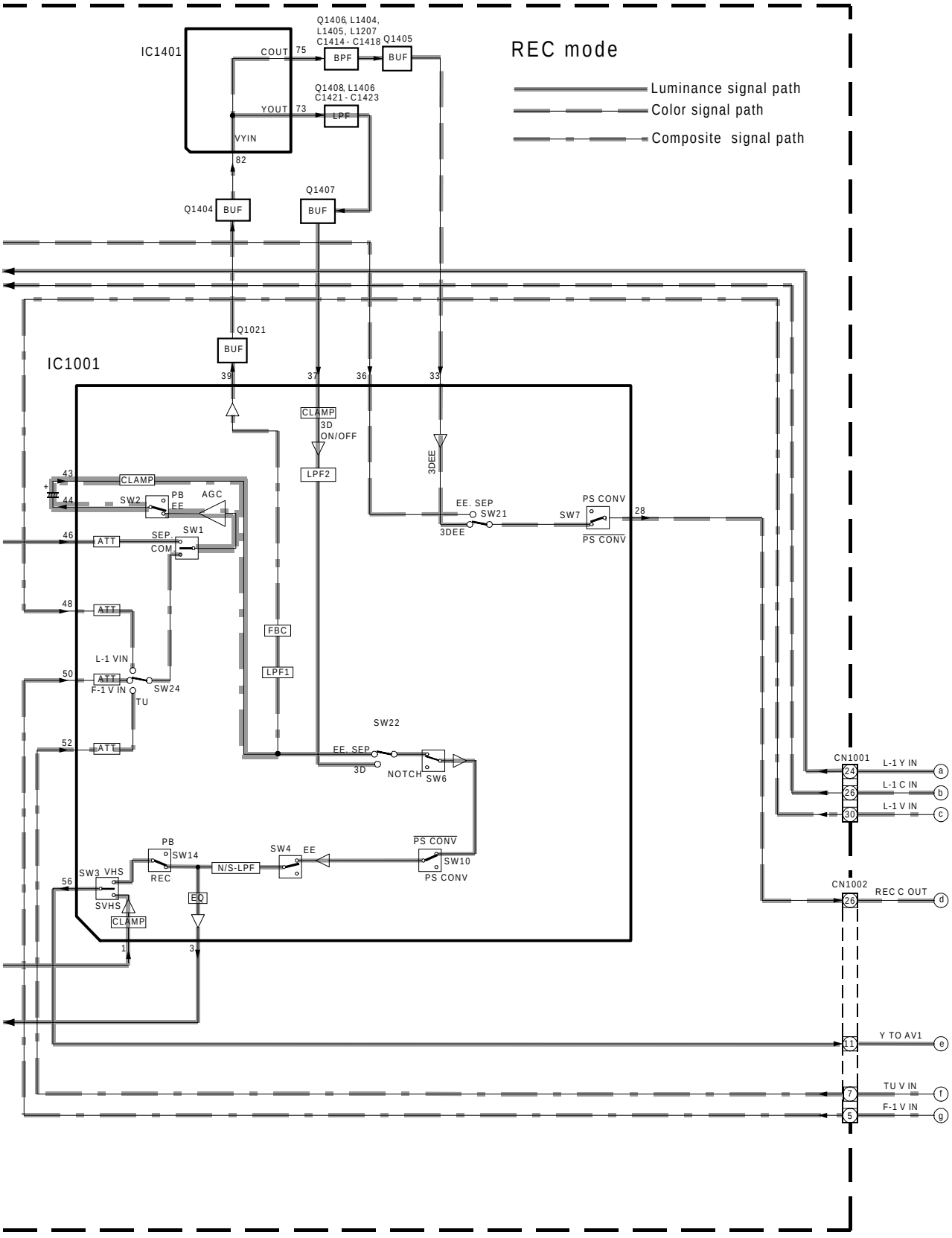

Fig. 1-2-1 Signal processing during recording (2/4)

· Signal processing during recording (3/4)

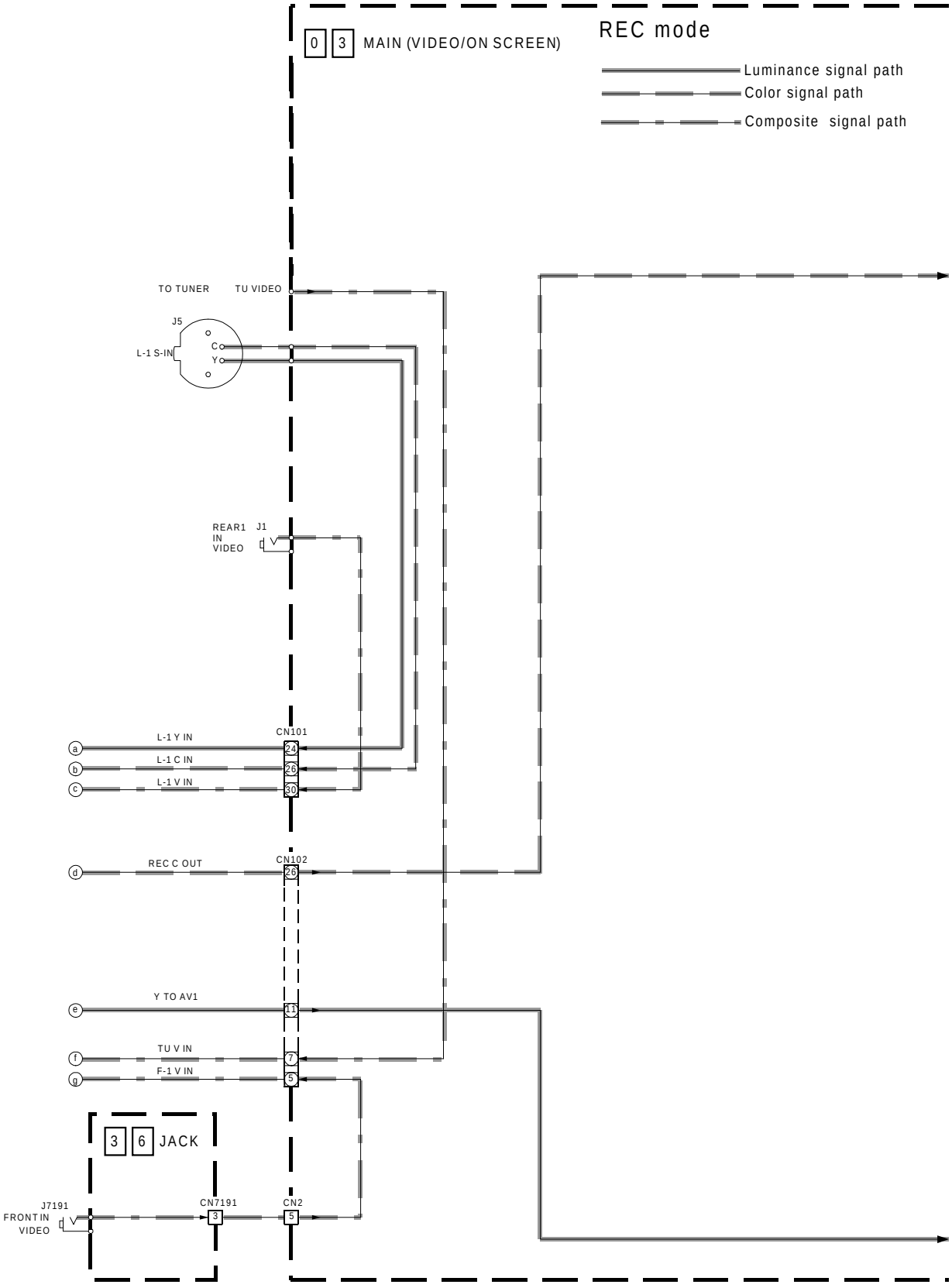

Fig. 1-2-1 Signal processing during recording (3/4)

· Signal processing during recording (4/4)

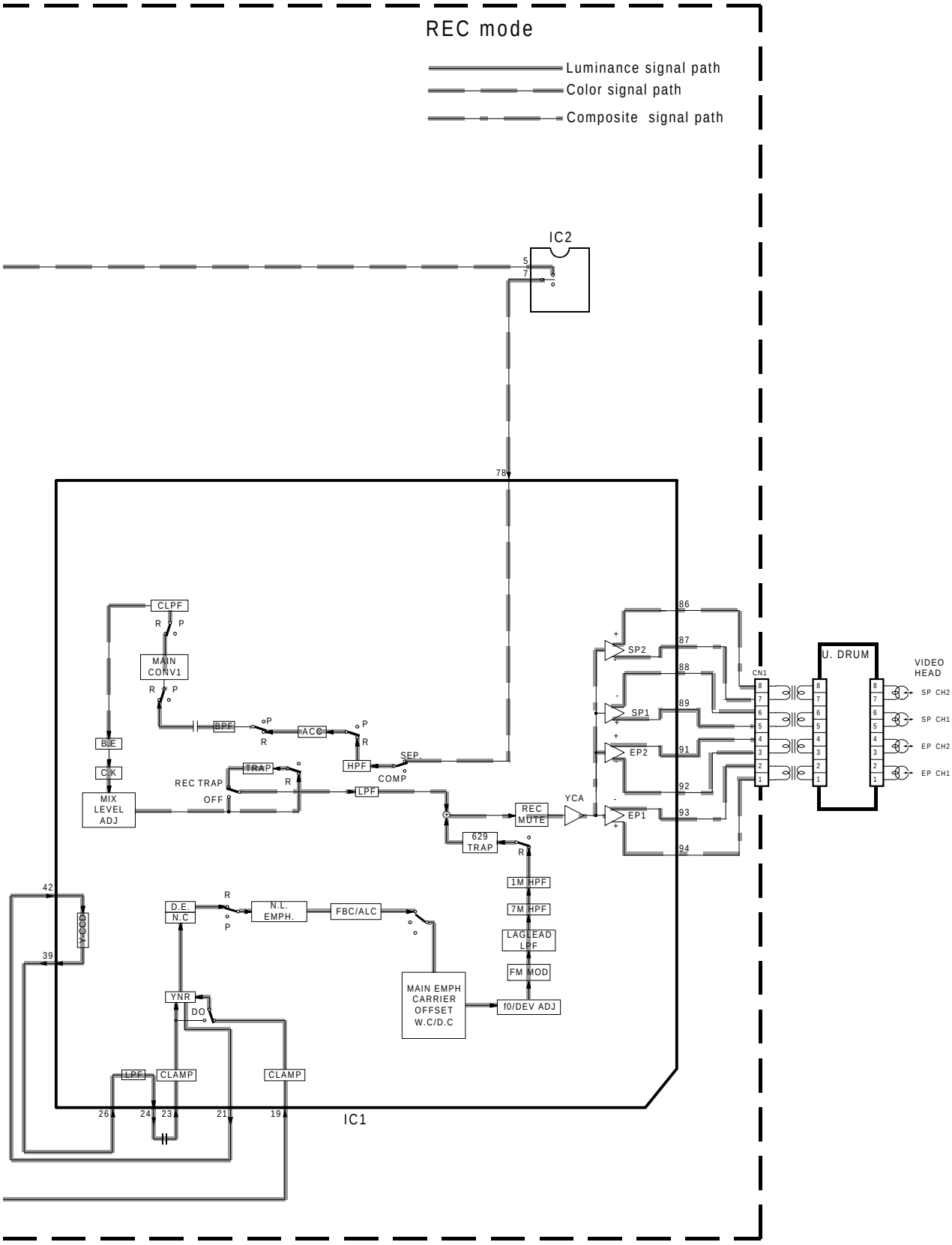

Fig. 1-2-1 Signal processing during recording (4/4)

· Signal processing during playback (1/4)

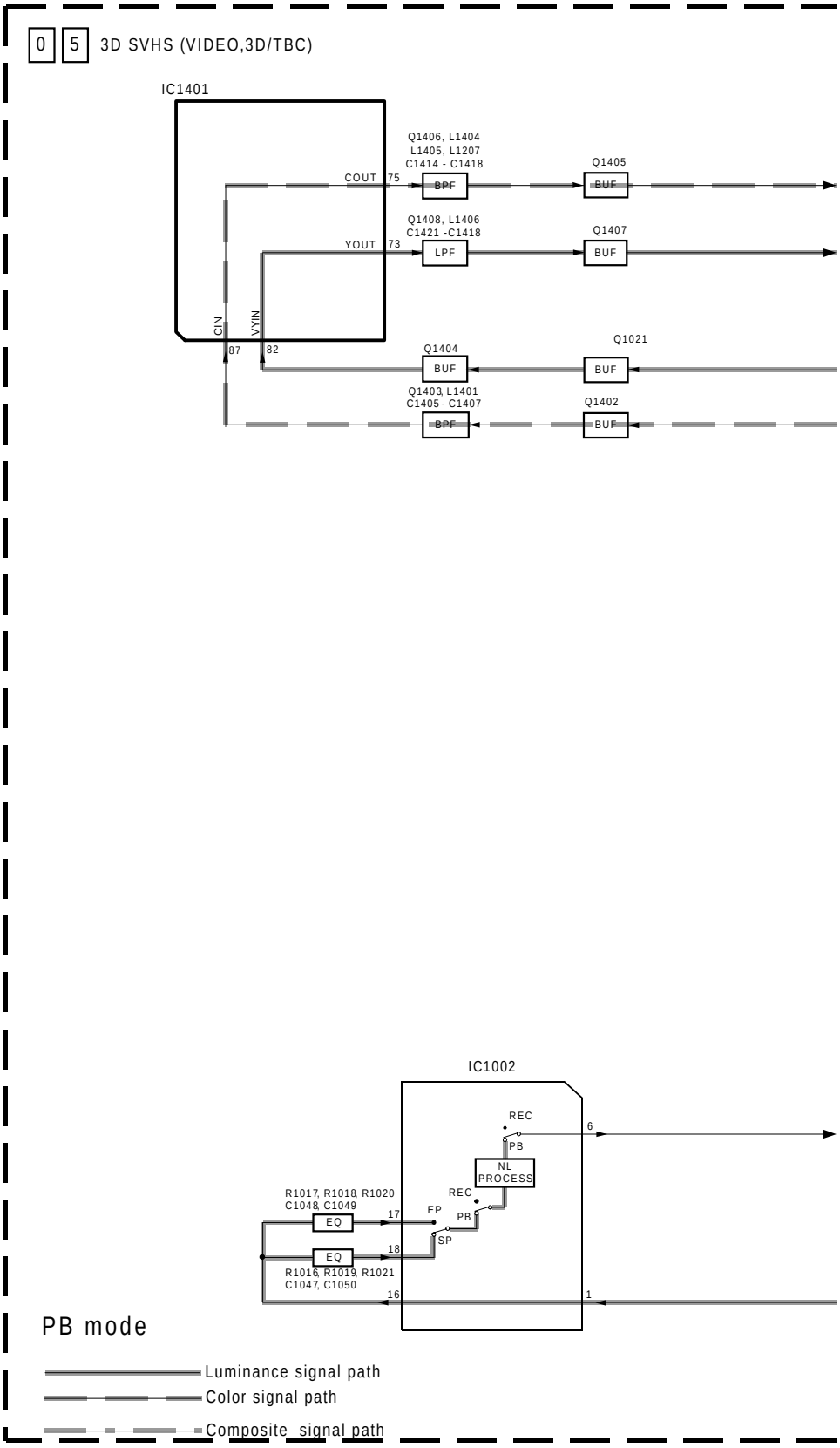

Fig. 1-2-2 Signal processing during playback (1/4)

· Signal processing during playback (2/4)

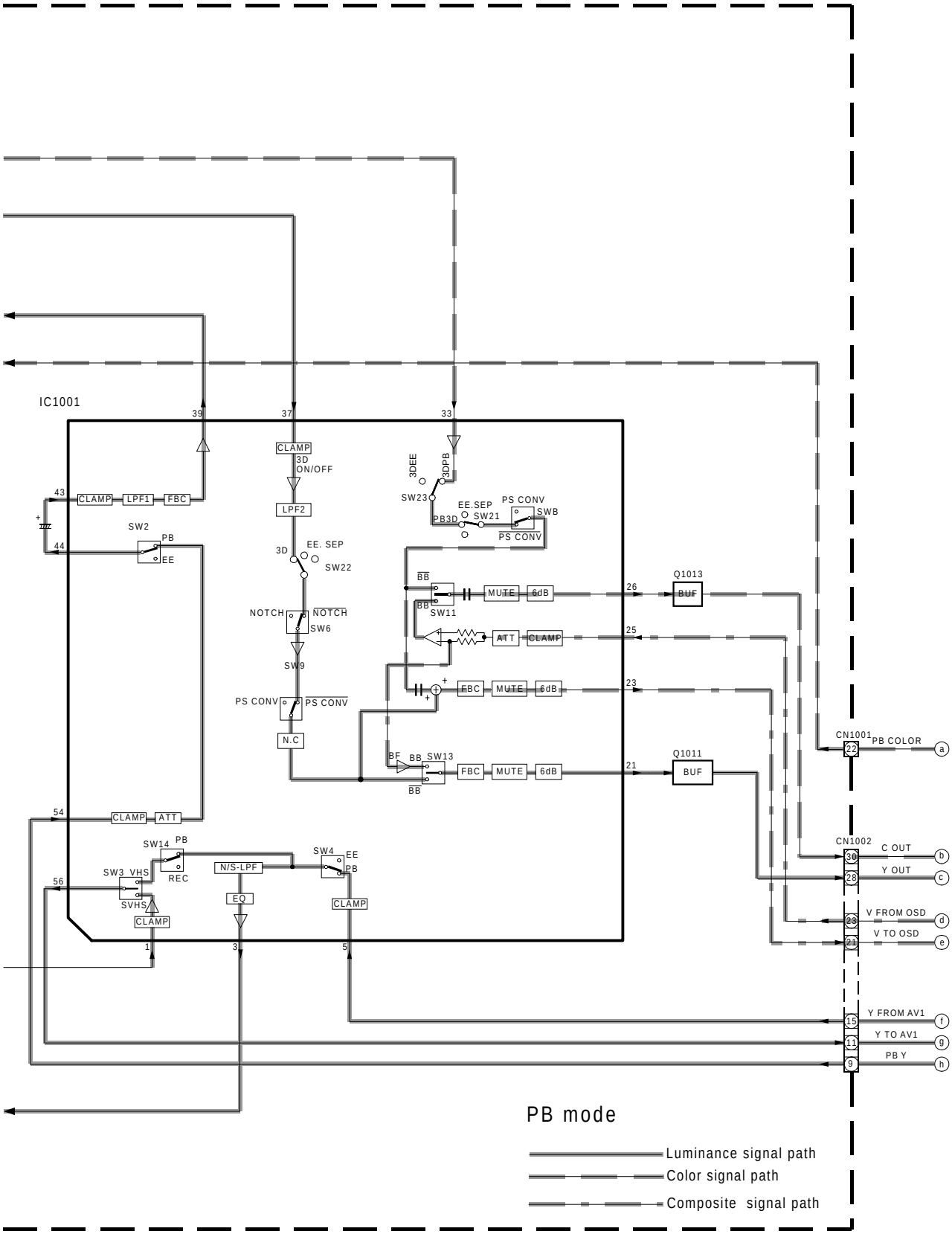

Fig. 1-2-2 Signal processing during playback (2/4)

· Signal processing during playback (3/4)

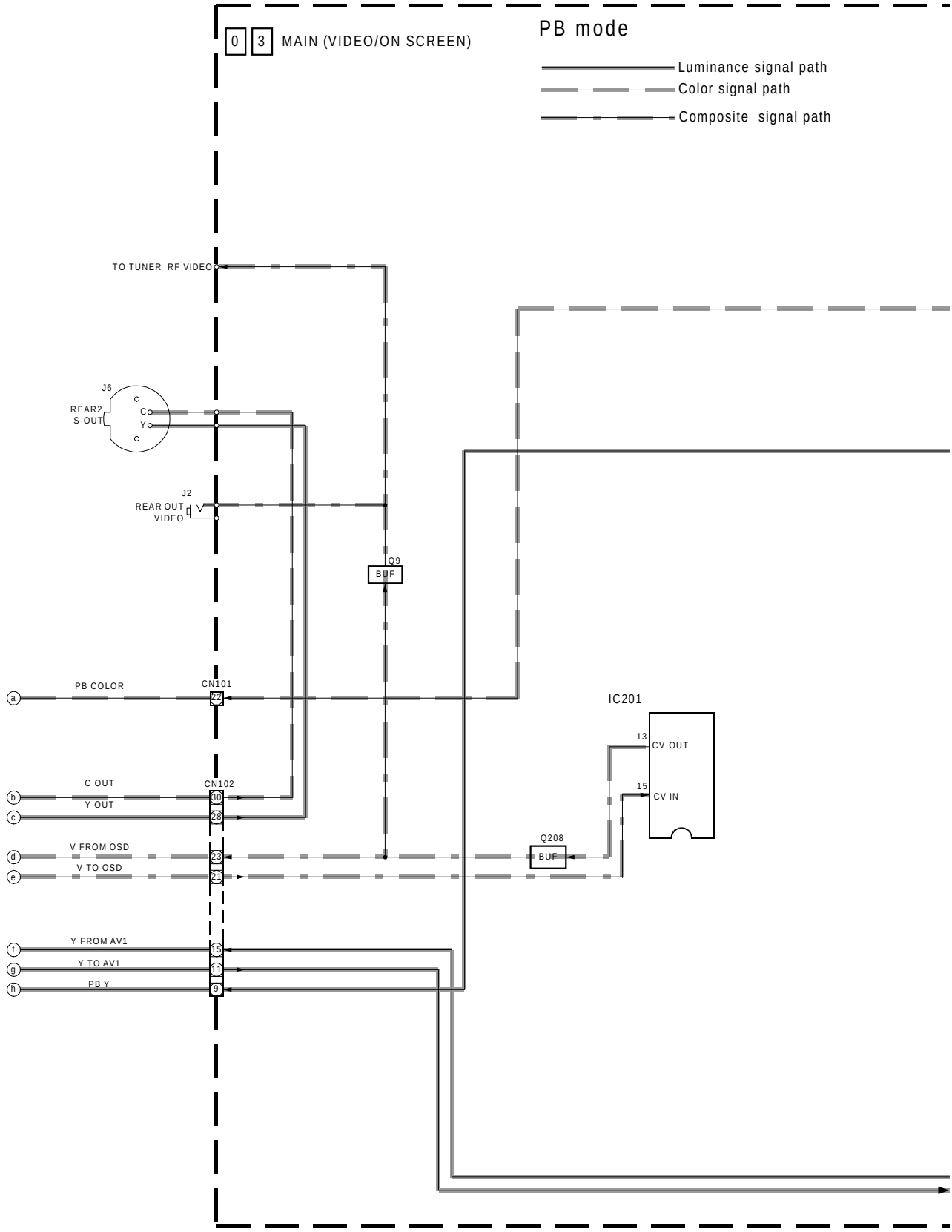

Fig. 1-2-2 Signal processing during playback (3/4)

· Signal processing during playback (4/4)

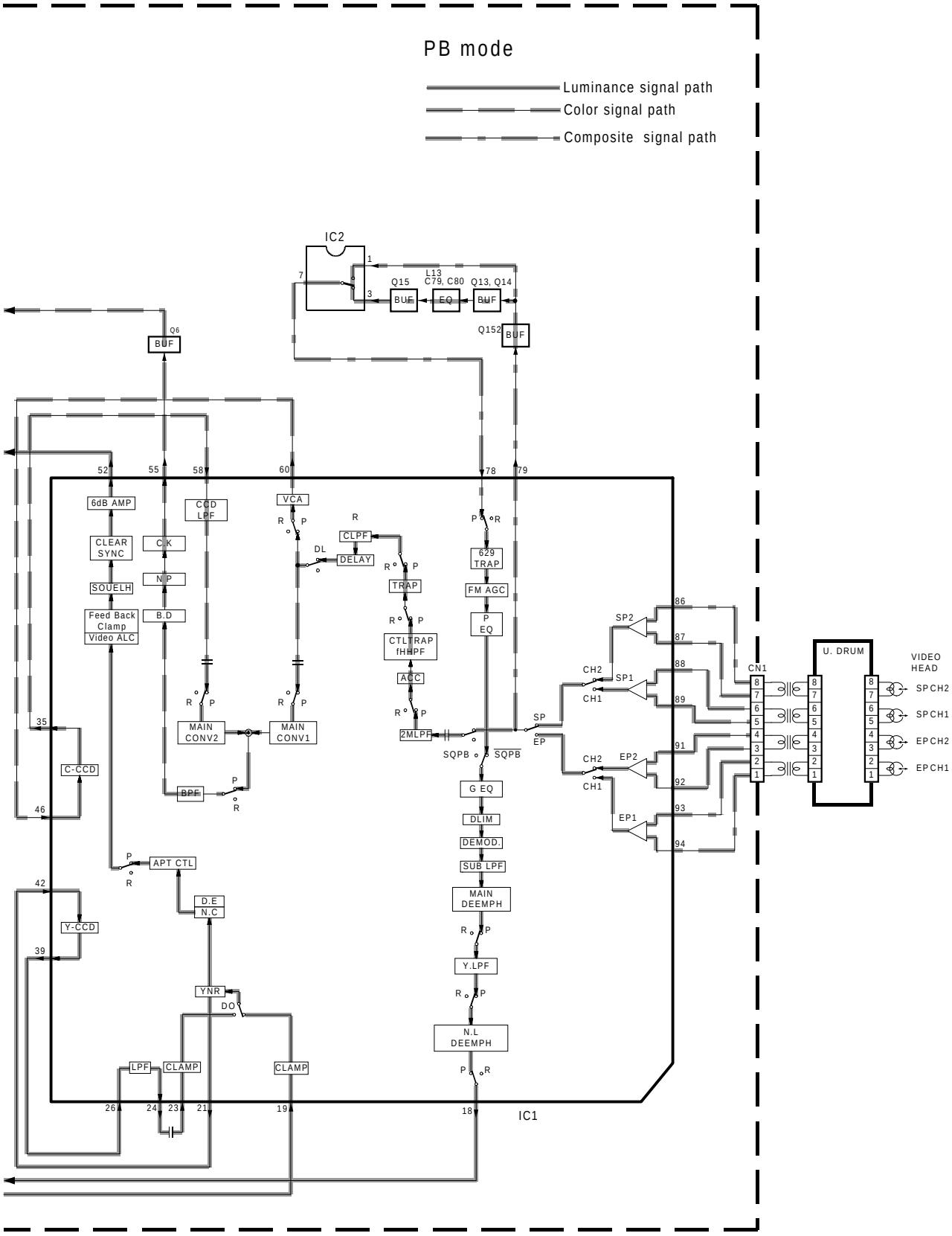

Fig. 1-2-2 Signal processing during playback (4/4)

· Signal processing during EE (1/2)

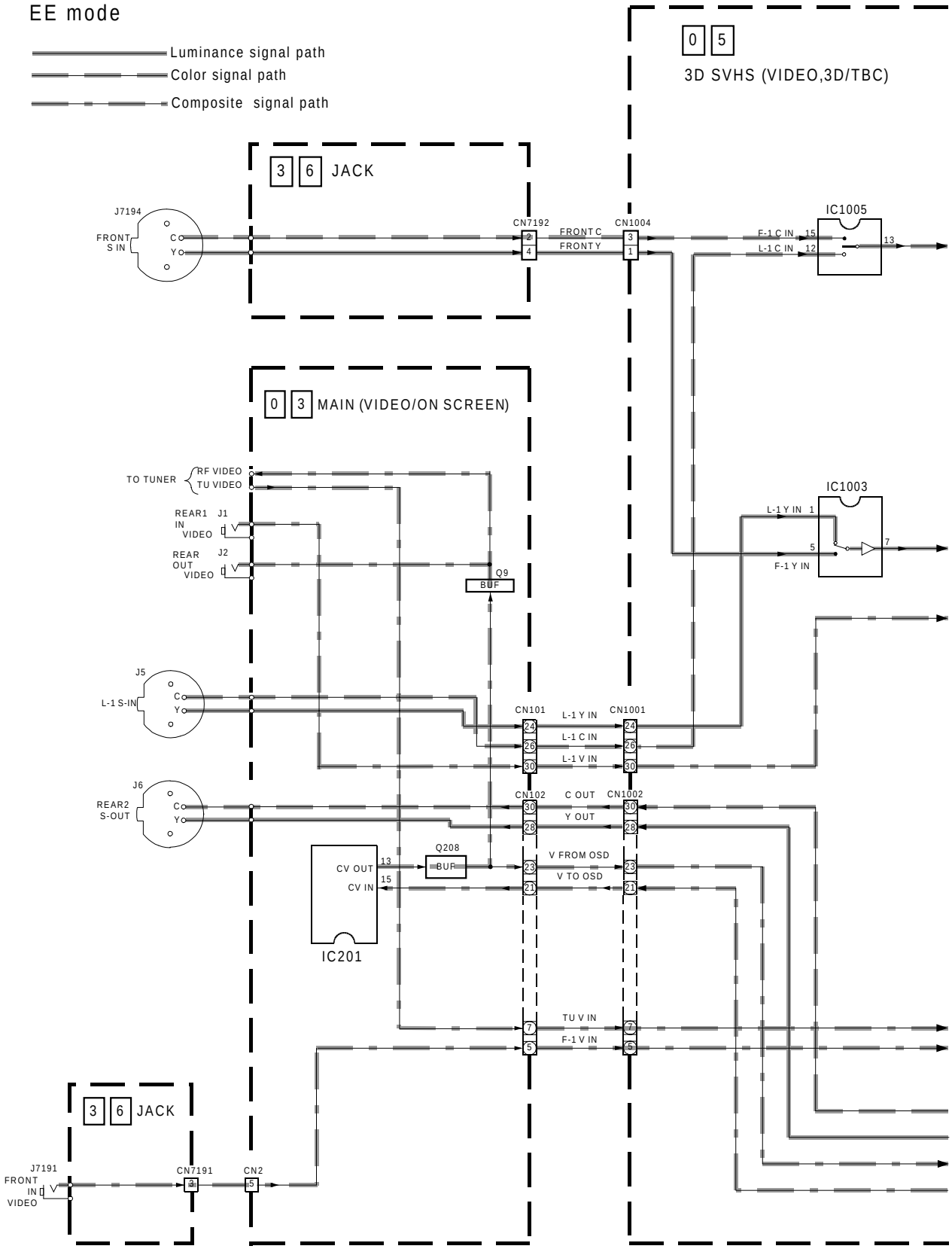

Fig. 1-2-2 Signal processing during EE (1/2)

· Signal processing during EE (2/2)

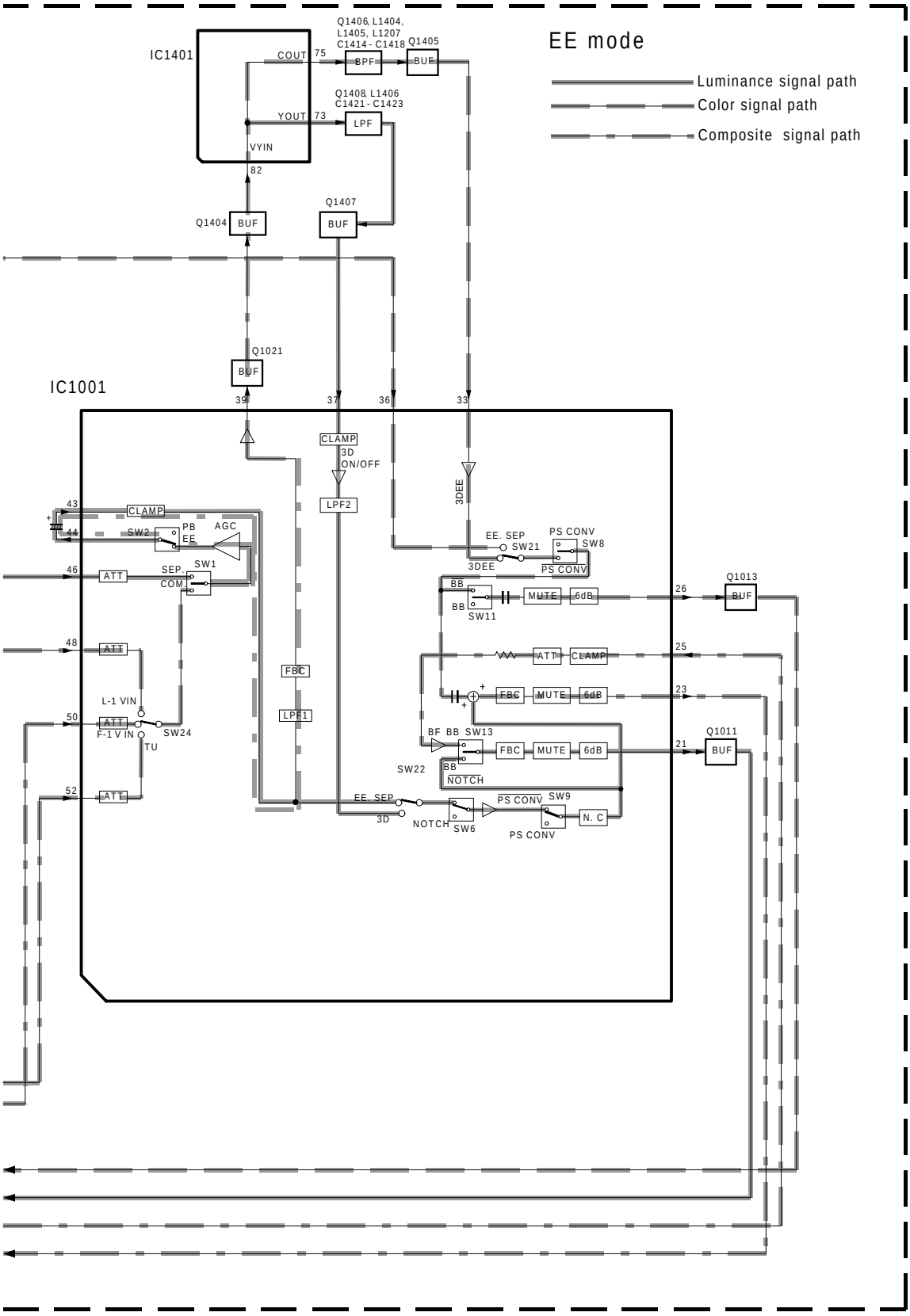

Fig. 1-2-2 Signal processing during EE (2/2)

1.3 THE SVHS ET FACILITY IN GENERAL

As is widely known, the SVHS ET facility is a new technique that enables SVHS recording and playback on a VHS tape. Note however that the SVHS ET facility is not an independent system but is just part of the SVHS system.

1.3.1 Hardware of the SVHS facility

As is seen from the block diagrams given in the previous sections for video signal processing in individual modes, there is no circuit dedicated to the SVHS ET system in the video circuitry. The SVHS ET facility basically shares its functions with the SVHS system circuit.
This means that it is not possible to install the SVHS ET facility in any model not equipped with an SVHS system. This is because the SVHS ET facility is part of the SVHS system as discussed above.
As is known, it is possible to record a VHS tape in the SVHS mode if an S detection hole is provided on the cassette shell. Since a VHS tape is of ferrous oxide just like an SVHS tape, there is no problem of inferior picture and sound quality if a VHS tape of superior magnetic characteristics is used for SVHS recording and playback.
However, since the SVHS ET facility is to be marketed as a commercial item, we have to satisfy the following two requirements.

1) SVHS ET format recording and playback should be guaranteed for all the tapes within the range of magnetic characteristics specified for the VHS format;
2) Playback of the tape recorded in the SVHS ET is ensured on all the existing SVHS models.

To accomplish this, the SVHS-format video circuit equipped with the SVHS ET facility offers the solutions described below when it is in the SVHS ET mode.

1) Change of the W/D clip level (recording circuit)
2) Change of the main emphasis characteristics (recording circuit)
3) Change of recording level (Y and C) and recording current (recording circuit)

While the details of each process are certainly important, the critical point here is that all the solutions are limited only to the recording circuit.
In other words, the playback circuit of the SVHS ET function is exactly the same as the SVHS system's playback circuit.

The SVHS ET facility meets the second requirement with its own specifications.
Besides, all these solutions are provided to achieve the second requirement on the presumption that the SVHS format's playback circuit is used for playback in the SVHS ET mode.
The details of those solutions are discussed below.

1) Change of the W/D clip level (recording circuit)
The VHS tape has inferior high-frequency characteristics to the SVHS tape. This may lead to a reversing effect during playback unless the white clip level (at the high-frequency range of the SVHS FM signal) is reduced. While, in the HR-S9500U, the white clip level in the SVHS mode is 210 % in the SVHS mode, it is 190 % in the SVHS ET mode.
Note however that this clip level is associated with the magnetic characteristics of heads and tapes, subsequent models may have a clip level different from the current setting.

2) Change of the main emphasis characteristics (recording circuit)
The main emphasis characteristics are also subjected to changes of frequency responses so that they comply with the characteristics of a VHS-format tape.

3) Change of recording level (Y, C) and recording current (recording circuit)
Regarding this subject, the tape used when writing the standard value of the best system of the IC1 pre-recording amp section is different between the SVHD ET mode and the SVHS mode (VHS tape in the SVHS ET mode and SVHS tape in the SVHS mode), the standard value is naturally different.
See the Technical Guide (VTG82081) of the HR-VP830U/E939EG/J936MS for details of the best system.

1.4 CPU PIN FUNCTIONS
1.4.1 IC1001 pin functions (1/2)

Pin No.	Pin Name	I/0	REF.
1	SUBEMPH	In	Subemphasis input
2	PB HI	-	REC/PB control
3	SUBEMPH	Out	Subemphasis output
4	COMB GAIN ADJ	-	Comb filter gain adjustment terminal
5	PB N/S LPF	In	N/S LPF input at PB mode
6	B.G.	-	Reference bias filter terminal
7	SW4	Out	N/S LPF input monitor terminal
8	S-VHS LOW	-	Current pull-in terminal at S-VHS mode
9	NOTCH TRAP	-	Notch trap filter terminal
10	CR DET	-	Smoothing filter pin of CR adjustment free circuit
11	fsc IN	In	fsc input terminal
12	VCA GAIN ADJ	-	VCA gain adjustment terminal
13	IIC DATA	In	Serial control data input
14	IIC CLOCK	In	Serial control clock input
15	SECAM CONV. DL	Out	SECAM delayline drive terminal
16	SECAM CONV. DL	In	Input terminal from SECAM delayline
17	NTSC HI	-	NTSC/PAL mode output control terminal (NTSC: 4V, PAL: 0V)
18	D TRAP	-	Dynamick trap terminal for noise cancelar
19	BLUE BACK TRAP	-	Trap filter terminal of blueback circuit
20	GND	-	Ground
21	Y	Out	Luminance signal output
22	FBC Y	-	Feedback filter terminal for luminance signal
23	V	Out	Composite video signal output terminal
24	OSD	-	OSD mute control terminal
25	BLUE BACK	In	Input terminal of video signal for blue back
26	C	Out	Color signal output
27	FBC V	-	Feedback filter terminal for video signal
28	REC C O	Out	REC color signal output

Table 1-4-1 IC1001 pin functions (1/2)

· IC1001 pin functions (2/2)

Pin No.	Pin Name	I/0	REF.
29	SECAM CONV.	In	Input terminal from SECAM converter
30	C OUT BIAS	-	Color signal bias control terminal
31	SECAM CONV.	Out	Output terminal to SECAM converter
32	V PULSE	In	V. Y mute control terminal
33	PB C	In	Playback color signal input
34	Vcc2	-	Power supply
35	REC C I	In	REC color signal input
36	COMB PHASE ADJ	-	Comb filter phase adjustment terminal
37	CCD	In	Input terminal from CCD
38	C ADJ BYPASS	-	Comb filter bypass terminal
39	LPF1	Out	LPF1 output terminal
40	FBC DET	-	Feedback filter terminal for video signal (LPF1)
41	CCD	Out	Output terminal to CCD
42	BPF TRAP	-	BPF trap filter terminal
43	MAIN CLAMP	In	Main clamp input terminal
44	MAIN CLAMP	Out	Output terminal to main clamp
45	DIGITAL LOW	-	Digital mode control terminal
46	Y	In	Luminance signal input controlled by SSB
47	AGC DET	-	Detection fliter terminal for AGC
48	V IN1	In	Input terminal of LINE and TUNER video controlled by SSB
49	Vcc	-	Power supply
50	V IN2	In	Input terminal of LINE and TUNER video controlled by SSB
51	SP HI	-	SP/EP control terminal
52	V IN3	In	Input terminal of LINE and TUNER video controlled by SSB
53	ALC CURRENT	-	Current output terminal for ALC
54	PB Y	In	Playback luminance signal input
55	YC MUTE	-	Input terminal for luminance and color signal mute
56	N/S LPF	Out	Output terminal VHS/S-VHS LPF

Table 1-4-1 IC1001 pin functions (2/2)

1.4.2 IC1 pin functions (1/3)

Pin No.	Pin Name	I/0	REF.
1	AUDIO PB IN (-)	In	Playback audio EQ amp feedback terminal
2	AUDIO PB IN (+)	In	Playback audio EQ amp input
3	AUDIO PB EP SW	In	PB: Audio playback EQ changeover switch
4	AUDIO REC OUT	Out	Recording audio output
5	AUDIO GND	-	Audio exclusive ground
6	AUDIO ALC FILTER	-	Audio ALC filter
7	ADUIO LINE IN3	In	Audio line input 3
8	ADUIO LINE IN2	In	Audio line input 2
9	AUDIO LINE IN1	In	Audio line input 1
10	AUDIO BYPASS	-	Bypass condenser terminal for DC regeneration
11	AUDIO LINE OUT	Out	Audio line output
12	Y-Vcc	-	Vcc for Y-system
13	MAIN EM OUT / MAIN DEEM IN	In/Out	Main emphasis feedback ouptut terminal at REC / Filter drive terminal of main deemphasis at PB
14	MAIN EM NF / MAIN DEEM OUT	In	Main emphasis feedback input terminal at REC / Input terminal after main deempasis filter at PB
15	f0 / DEV S-DET	-	Filter terminal for adjustment free of f0 and deviation for REC FMMOD PB VHS/S-VHS discrimination filter terminal
16	E-PEAK	-	Filter terminal for main deemphasis emitter peaking
17	G-EQ SB ADJ	-	Low characteristics adjustment terminal for FM signal
18	CLAMP DRIVE	-	Y signal pass route
19	MAIN CLAMP IN	In	Main clamp input terminal (To Sync sep. YNR, AGC DET)
20	REC ME FBC / PB APL	-	Main emphasis FBC filter at REC / Main deemphasis APL filter at PB
21	Y-CCD DRIVE	Out	Y-CCD drive output terminal
22	ME ALC / PB FM AGC	-	Filter for level adjustment free of main emphasis part / Adjustment free filterof playback FM level
23	Y-CCD CLAMP	In	Clamp input terminal for Y-CCD LPF output
24	Y-CCD LPF OUT	Out	Y-CCD LPF output
25	CCD ADJ	-	Level difference detection terminal to correct CCD gain fluctuation
26	FROM Y-CCD	In	Y-CCD feedback LPF input
27	Y GND	-	GND for Y-system
28	LINE 3 IN	In	Input terminal of LINE and tuner video controlled by I2C
29	AGC DET	-	Detection filter terminal for video AGC
30	LINE 2 IN	In	Input terminal of LINE and tuner video controlled by I2C
31	LINE 1 IN	In	Input terminal of LINE and tuner video controlled by I2C
32	NC	-	Not used
33	NC	-	Not used

Table 1-4-2 IC1 pin functions (1/3)

· IC1 pin functions (2/3)

Pin No.	Pin Name	I/0	REF.
34	NC	-	Not used
35	CCD C-OUT	Out	Chrominance signal output
36	CCD VCC	-	Not used
37	CCD MODE CTL	In	Mode select (L: PAL/SECAM, M: 4.43NTSC H: NTSC 3.58))
38	NC	-	Not used
39	CCD Y-OUT	Out	Luminance signal output
40	NC	-	Not used
41	NC	-	Not used
42	CCD Y-IN	In	Luminance signal input
43	NC	-	Not used
44	CCD CLOCK	In	Clock input
45	CCD GND	-	Not used
46	CCD C-IN	In	Chrominance signal input
47	NC	-	Not used
48	NC	-	Not used
49	NC	-	Not used
50	SYNC SEP OUT	Out	Sync. sepa. output
51	SQUELCH IN	In	Squelch input terminal
52	VIDEO OUT	Out	Video output terminal for EE, PB
53	VIDEO OUT F.B.C	-	FBC filter
54	COLOR IN	In	Playback C mix input terminal
55	PB C OUT	Out	C out of playback output terminal
56	VIDEO OUT ALC	-	Adjustment free filter terminal for EE and PB video output level
57	CCD CONT	-	CCD mode outupt control terminal
58	C-CCD FB IN	In	C CCD feedback input terminal
59	LEVEL DET	-	Level detect smoothing filter pin
60	C-CCD DRIVE	Out	C CCD drive terminal
61	C Vcc	-	Vcc for C system
62	IIC CLK	In	Serial control clock input terminal
63	IIC DATA	In	Serial control data input terminal
64	KILLER OUT	Out	Killer detect output terminal
65	2fsc VCO DET	-	2fsc filter terminal
66	LC VCO	-	LC terminal for VCO

Table 1-4-2 IC1 pin functions (2/3)

· IC1 pin functions (3/3)

Pin No.	Pin Name	I/0	REF.
67	VIDEO OUT VCC	-	Vcc for Video out
68	C-GND	-	GND for color system
69	CCD SIG 2fsc OUT	Out	Clock output pin for CCD
70	CR DET	-	Smoothing filter pin of CR adjustment free circuit
71	3.58 X-TAL IN	In	3.58 NTSC crystal OSC input terminal
72	ACC DET	-	Burst ACC detection filter terminal
73	X-TAL OSC OUT	Out	Crystal OSC driving terminal
74	REC APC	-	Recording APC filter terminal
75	3.58/4.43X-TAL IN	In	Crystal OSC input terminal of PAL, M-PAL, N-PAL and 4.43 NTSC
76	PB APC REC AFC	-	Recording AFC filter playback APC filter terminal
77	DET FOR DISCRI.	-	MESECAM for detection filter terminal
78	REC SEP C IN / PB SIG IN	In	Recording sepalation color input
79	PB C OUT	Out	Pre amp output pin at PB mode
80	SP/EP HEAD SELECT	-	SP/EP head select signal pin
81	DRUM FF IN	In	Drum FF input
82	CK DET	-	Color killer detection filter terminal
83	DISCRI	-	Discrimination filter pin for recording / playback which controls LCVCO
84	ENV OUT	Out	PB FM envelope detect output
85	PRE REC MAIN GND	-	GND for PRE/REC
86	SP CH2 PLUS	In/Out	PRE amp input / REC amp output (current output)
87	SP CH2 MINUS	In/Out	PRE amp input / REC amp output (current output)
88	SP CH1 MINUS	In/Out	PRE amp input / REC amp output (current output)
89	SP CH1 PLUS	In/Out	PRE amp input / REC amp output (current output)
90	PRE/REC Vcc	-	Vcc for PRE/REC
91	SP(L) CH2 PLUS	In/Out	PRE amp input / REC amp output (current output)
92	SP(L) CH2 MINUS	In/Out	PRE amp input / REC amp output (current output)
93	SP(L) CH1 MINUS	In/Out	PRE amp input / REC amp output (current output)
94	SP(L) CH1 PLUS	In/Out	PRE amp input / REC amp output (current output)
95	B.G.	-	Reference bias filter terminal
96	AUDIO Vcc	-	Vcc for audio system
97	S-VHS ET DISCRI	Out	Output mode
98	DO OUT	Out	DO output
99	AUDIO MUTE	-	Audio mute
100	AUDIO PB EQ OUT	Out	Playback audio EQ amp output for feedback

Table 1-4-2 IC1 pin functions (3/3)

SECTION 2
3D VIDEO CIRCUIT

2.1 3 DEMENSION VIDEO SIGNAL PROCESSOR SYSTEM

Let us discuss signal processing in general taking the HR-S9500U as an example.

2.1.1 3 dimension video signal processor system block diagram

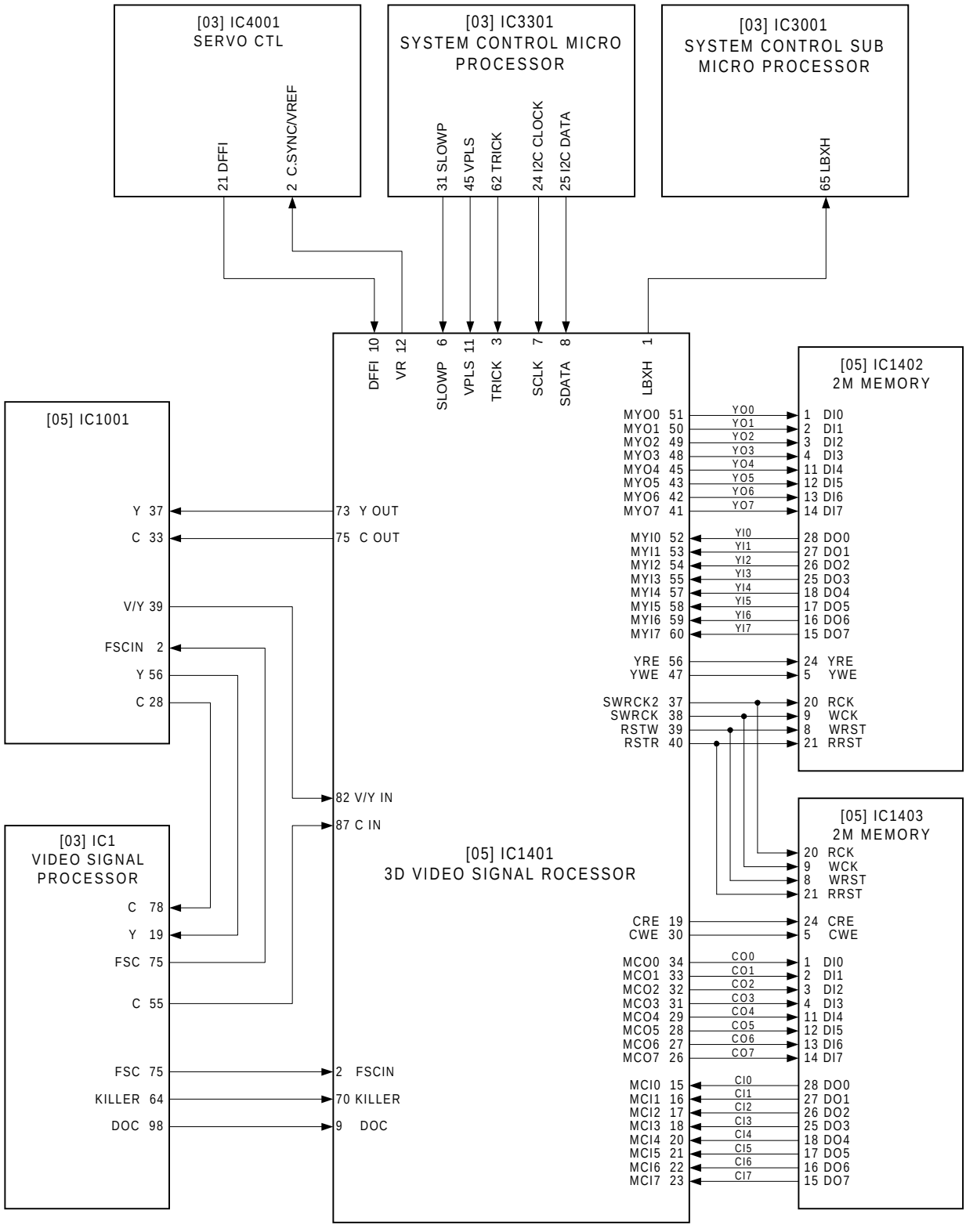

Fig. 2-1-1 3 dimension video signal processor system block diagram

2.2 EXPLANATIONS OF 3 DEMENSION VIDEO SIGNAL PROCESSOR LSI

2.2.1 EE/REC mode

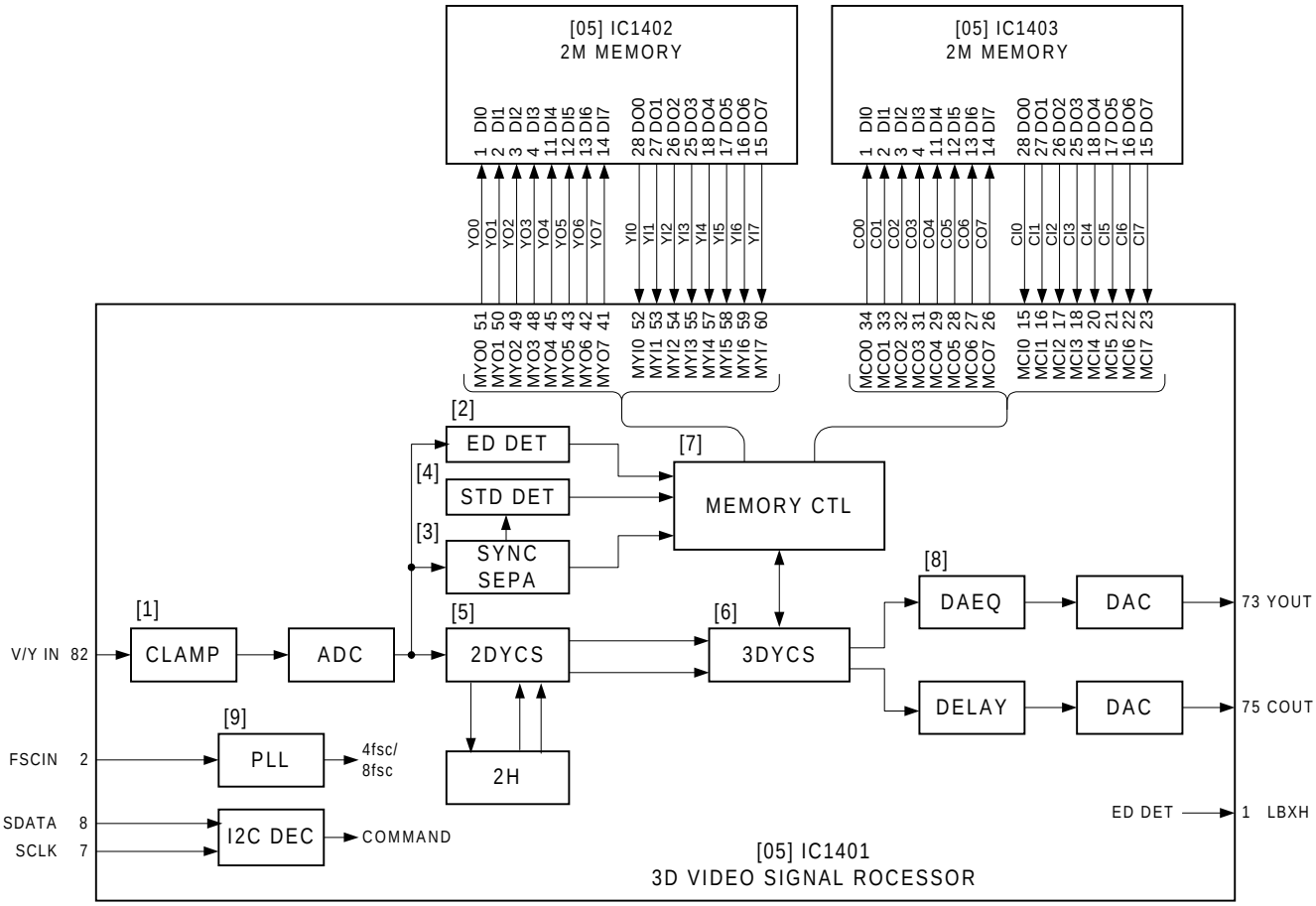

Fig. 2-2-1 EE/REC mode block diagram of 3D video signal processor

1. CLAMP

This sync tip clamp improves response and defect of sync tip as a result of reconsideration of change in clamping current.

2. ED DET

In the EE mode LETTER BOX SQUEEZE DETECTION is activated to detect letter box squeeze with 22H EDTV II DISCRIMINATION signal. In the letter box PB mode LETTER BOX BLANK PART MUTE is activated to mute blank part by serial control or NR OFF functions to turn off NR system.

3. SYNC SEPARATION

Extracts SYNC signal in accordance with synchronous tip.

4. NON-STANDARD DETECTION (STD DET)

In the EE mode signals unconformable to the NTSC standard are detected by this circuit.

5. 2DYCS (2D YC SEPARATION)

The logic comb system is adopted for NTSC while the logic system is adopted for PAL and M-PAL. The NTSC, PAL and M-PAL have the horizontal median control (on/off).
One-dimensional processing in the N-PAL and SECAM modes.

6. 3DYCS

Motion detection sensitivity can be set in three steps: near animation, standard, and near still. Switching from 2-D to 3-D can be set in five steps.

7. MEMORY CONTROL

1) Memory control vertical timing adjustment

Vertical timing adjustment is effective only for memory write timing in the trick mode and it is adjustable between -7H and +7H. Adjustment of time lag in V. pulse during DD playback can be manually corrected.

2) Lower part mute in digital trick

The lower part of picture is muted into black in the digital trick mode. Mute width is variable for 9H, 12H or 15H in the bottom of picture.

3) 3D NR in DD PB

This circuit activates the three-dimensional NR system in the DD PB mode as same as the normal PB mode. However, this 3D NR is not activated in the digital trick mode in which the memory is used for trick operation.

4) Non-interlace in continuous slow operation

In the digital trick mode, continuous slow operation is smoothly performed by this function because it processes signal without interlacing.

5) 1H V hold correction by V pulse

When V. pulse is used as the vertical reference, V hold may be unstable for 1H because of jitter of the signal. This circuit functions to correct such the unstable V hold.

8. DA EQUALIZER

Corrects frequency response of the DA converter with the digital filter.

9. PLL (MULTICLOCK PLL)

This circuit oscillates clock of the burst clock by comparing the phase of input fsc with that of sine wave read out of the ROM according to the broadcasting system. Oscillation frequency that conforms to fsc of each broadcasting system is 8 fsc or 4 fsc.

2.2.2 PB mode

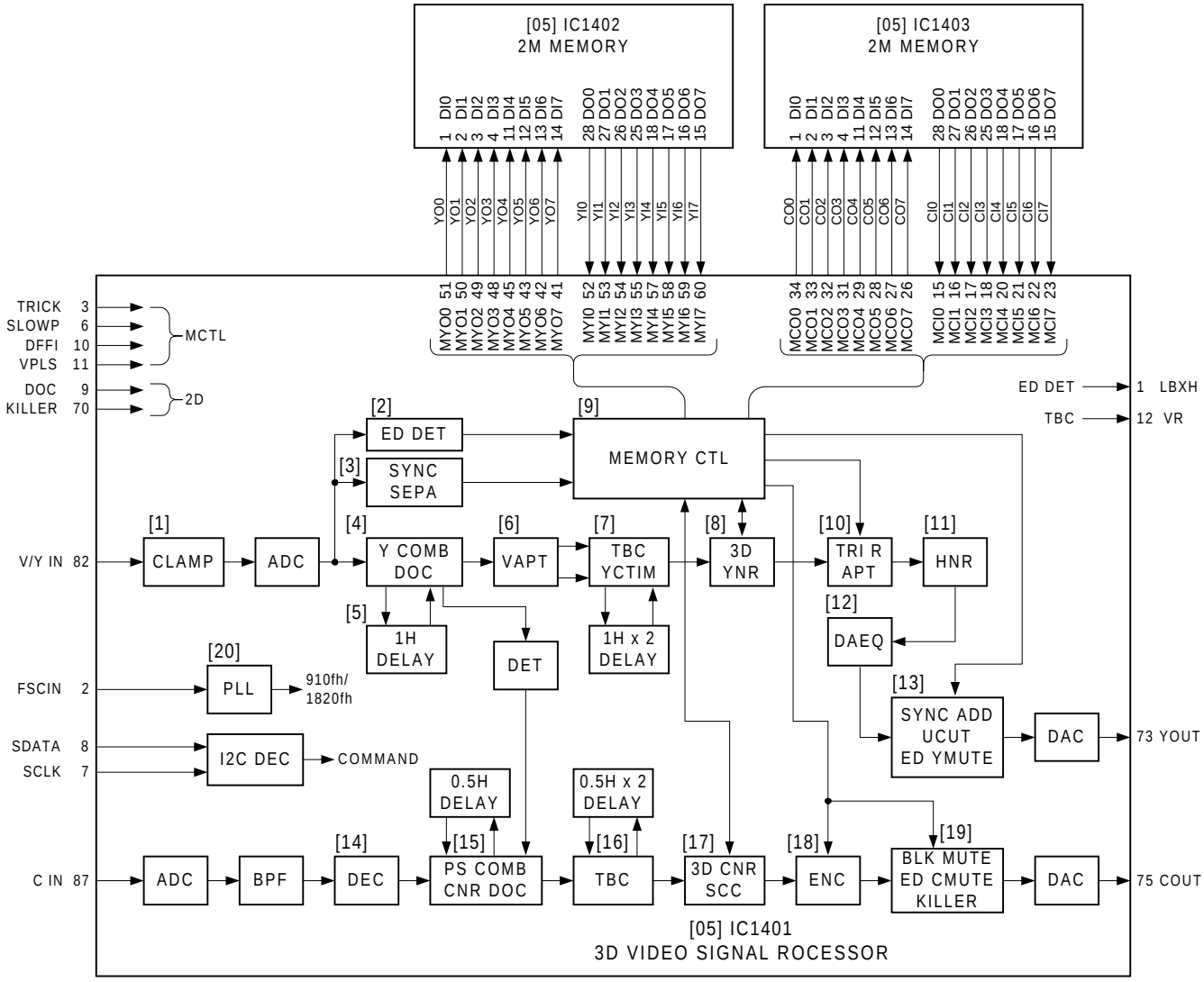

Fig. 2-2-2 PB mode block diagram of 3D video signal processor

1. CLAMP

This sync tip clamp improves response and defect of sync tip as a result of reconsideration of change in clamping current.

2. ED DET

In the EE mode LETTER BOX SQUEEZE DETECTION is activated to detect letter box squeeze with 22H EDTV II DISCRIMINATION signal. In the letter box PB mode LETTER BOX BLANK PART MUTE is activated to mute blank part by serial control or NR OFF functions to turn off NR system.

3. SYNC SEPARATION

Extracts SYNC signal in accordance with synchronous tip.

4. Y COMB/DOC

1) Y COMB

The Y comb filter actuated in the PB mode. Limiter width can be varied in three steps.

2)DOC

Outputs dropout-compensated Y and C signals in the PB mode by adding a signal 1H before each dropout to the signal.

5. Y1H DELAY

Delays Y signal by 1H in the PB mode to reduce color blurring caused by the PS comb.

6. VAPT

The vertical aperture in the PB mode. Although the vertical aperture is interlocked with the APT (horizontal aperture) in previous IC's, this VAPT is variable individually.

7. TBC/YCTIM

1) TBC

This TBC is an interpolating TBC that operates with single clock. While correcting jitter within +/-1H by the 2H line memory, this TBC prevents the memory from overflowing by servo control based on readout of the memory.

2) YC timing adjustment

Adjusts YC timing in the range between -4T and +3T.

8. 3DYNR

A frame cyclic NR circuit to improve S/N ratio of luminance signal in the PB mode. Residual image is reduced by hadamard conversion and dynamic vector correction. Reduction effect can be set in 7 steps besides OFF. Improvement rate is 0 to 8.4 dB (when TBC is on) or 0 to 1.4 dB (when TBC is off).

9. MEMORY CTL

1) Memory control vertical timing adjustment

Vertical timing adjustment is effective only for memory write timing in the trick mode and it is adjustable between -7H and +7H. Adjustment of time lag in V. pulse during DD playback can be manually corrected.

2) Lower part mute in digital trick

The lower part of picture is muted into black in the digital trick mode. Mute width is variable for 9H, 12H or 15H in the bottom of picture.

3) 3D NR in DD PB

This circuit activates the three-dimensional NR system in the DD PB mode as same as the normal PB mode. However, this 3D NR is not activated in the digital trick mode in which the memory is used for trick operation.

4) Non-interlace in continuous slow operation

In the digital trick mode, continuous slow operation is smoothly performed by this function because it processes signal without interlacing.

5) 1H V hold correction by V pulse

When V. pulse is used as the vertical reference, V hold may be unstable for 1H because of jitter of the signal. This circuit functions to correct such the unstable V hold.

10. TRI R/APT

1) APT

The horizontal aperture in the PB mode. Effect of this APT can be set in seven steps, namely 3 steps in the softening side, neutral (center) and 3 steps in the sharpening side. The TRI R is employed for the sharpening side.

2) TRI R

The detail enhancer, which gives picture more natural sharpness because it sharpens edges without excessive overshoot. Enhancing effect of the TRI R is variable in four degrees: feeble, weak, intermediate and strong, independently from the VAPT.

11. HNR

One-dimensional hadamard noise reduction circuit. This noise reduction function can be set in three modes of low, middle and high besides OFF, and limiter level in each mode can be switched between high and low.

12. DEC (DECODER)

Demodulates chroma signal into color difference signal in the PB mode with the TBC turned on. Sensitivity is changeable by varying threshold level of the feed forward APC.

13. PS COMB/2D CNR

1) PS Comb

The two-line comb filter, which also serves as a three-line comb filter in combination with the PS comb filter built in IC1. This comb filter takes effect when the TBC is on in the PB mode.

Since this filter shares the line memory with the PS comb filter, it functions as a CNR circuit together with the PS comb filter. For reducing data to be saved in the memory, data on the cyclic route is curtailed (interlaced) by half in this circuit. There are two cyclic coefficients, namely 0.5 and 0.75.

2) DOC

Outputs dropout-compensated Y and C signals in the PB mode by adding a signal 1H before each dropout to the signal.

17. 3DCNR/SCC

The CNR of this circuit is a combination type of frame cyclic CNR and frame non-cyclic CNR, and its reduction effect can be set in 7 steps besides OFF. The SCC emphasizes high components by frame cyclic processing (in 3 steps) as well as emphasizes edges by horizontal direction processing.

18.ENC (ENCODER)

Modulates color difference signal into chroma signal. Color thickness (tint and shade) can be adjusted by the newly adopted function that increases variable burst level by 20 %.

19. BLK MUTE/ED MUTE/KILLER

1) Color blank mute

In the PB mode, unnecessary color signals in the horizontal blanking periods and PAL pilot burst signals are muted by this circuit, which also functions to reduce transverse noise.

2) killer

Mutes color signal while receiving KILLER pulse in the PB mode.

20. PLL (MULTICLOCK PLL)

This circuit oscillates clock of the burst clock by comparing the phase of input fsc with that of sine wave read out of the ROM according to the broadcasting system. Oscillation frequency that conforms to fsc of each broadcasting system is 1820 fh or 910 fh.

2.3 LSI PIN FUNCTION

2.3.1 3D video signal processor LSI (IC1401) pin function (1/2)

Pin No.	Pin Name	I/0	REF.
1	LBXH	OUT	Letter box detect signal of EDTV II block
2	FSCIN	IN	fsc clock input
3	TRICK	IN	Trick control signal (Trick: high)
4	VDD	-	Power supply
5	VSS	-	Ground
6	SLOWP	IN	Memory write control signal (for trick mode) write: high
7	SCLK	IN	Serial data clock input
8	SDATA	IN	Serial data input
9	DOC	IN	Drop out control input (DOC: high)
10	DFFI	IN	Drum FF input
11	VPLS	IN	V pulse input (for vertical timing of trick mode)
12	VR	OUT	Reference signal from TBC
13	TCLK	IN	Clock input for test
14	CKMODE	IN	Clock mode select
15	MCI0	IN	Color memory data inputs (Form IC1403)
16	MCI1		
17	MCI2		
18	MCI3		
19	CRE	OUT	Color memory data read enable
20	MCI4	IN	Color memory data inputs (Form IC1403)
21	MCI5		
22	MCI6		
23	MCI7		
24	VDD	-	Power supply
25	VSS	-	Ground
26	MCO7	OUT	Color memory data outputs (To IC1403)
27	MCO6		
28	MCO5		
29	MCO4		
30	CWE	OUT	Color memory data write enable
31	MCO3	OUT	Color memory data outputs (To IC1403)
32	MCO2		
33	MCO1		
34	MCO0		
35	VDD	-	Power supply
36	VSS	-	Ground
37	SWRCK2	OUT	Serial read clock signal of luminance and color memory
38	SWRCK	OUT	Serial write clock signal of luminance and color memory
39	RSTW	OUT	Reset write signal of luminance and color memory
40	RSTR	OUT	Reset read signal of luminance and color memory
41	MYO7	OUT	Luminance memory data outputs (To IC4402)
42	MYO6		
43	MYO5		
44	VDD	-	Power supply
45	VSS	-	Ground
46	MYO4	OUT	Luminance memory data output (To IC1402)
47	YWE	-	Luminance memory data write enable
48	MYO3	OUT	Luminance memory data outputs (To IC1402)
49	MYO2		
50	MYO1		

Table 2-3-1 3D video signal processor LSI (IC1401) pin function (1/2)

· 3D video signal processor LSI (IC1401) pin function (2/2)

Pin No.	Pin Name	I/0	REF.
51	MYO0	OUT	Luminance memory data output (To IC1402)
52	MYI0	IN	Luminance memory data inputs (From IC1402)
53	MYI1		
54	MYI2		
55	MYI3		
56	YRE	OUT	Luminance memory data read enable
57	MYI4	IN	Luminance memory data inputs (From IC1402)
58	MYI5		
59	MYI6		
60	MYI7		
61	VDD	-	Power supply
62	VSS	-	Ground
63	TS1	IN	Test terminal (Normal: Low)
64	RST	IN	System reset terminal (Reset: Low)
65	MTO	IN	Test terminal (Normal: Low)
66	MON3	-	Not used
67	MON2	-	Not used
68	MON1	-	Not used
69	MON0	OUT	Monitor terminal
70	KILLER	IN	Killer circuit setting terminal
71	DFFO	-	Not used
72	AVDD	-	Analog circuit power supply
73	YOUT	OUT	Luminance signal analog output
74	AVSS	-	Analog circuit ground
75	COUT	OUT	Color signal analog output
76	COMP	IN	Capacitor terminal for phase compensation
77	IREF	OUT	Resistor terminal for bias current setting
78	VREF	IN	Reference voltage input
79	AVDD	-	Analog circuit power supply
80	AVSS	-	Analog circuit ground
81	CLAMP	OUT	Clamp correction terminal
82	YVIN	IN	Video signal or Luminance signal input
83	VRTV	IN	Reference voltage input for top side
84	VRTC	IN	Reference voltage input for top side
85	VRBV	IN	Reference voltage input for bottom side
86	VRBC	IN	Reference voltage input for bottom side
87	CIN	IN	Color signal input
88	AVDD	-	Analog circuit power supply
89	AVSS	-	Analog circuit ground
90	PVREF	IN	Reference voltage input
91	PIREF	OUT	Resistor terminal for bias current setting
92	PCOMP	IN	Capacitor terminal for phase compensation
93	AVDD	-	Analog circuit power supply
94	AVSS	-	Analog circuit ground
95	RFSC	OUT	fsc output (to external LPF)
96	PFSC	IN	fsc input (through the external LPF)
97	PCO	OUT	Phase detector output terminal
98	VCO	IN	VCO input terminal
99	AVSS	-	Analog circuit ground
100	AVDD	-	Analog circuit power supply

Table 2-3-1 3D video signal processor LSI (IC1401) pin function (2/2)

SECTION 3
SYSCON CIRCUIT

3.1 EXPLANATION OF SYSCON CIRCUIT

1998 models of JVC VCR's are roughly classified into two types: the first type has the CPU composed of one IC chip and the second type has the coupled CPU composed of two IC chips. Since the syscon system of 1998 models falling into the former type (having one-chip CPU) has nothing particularly different from that of the models for the previous years, the following explains the syscon system of the second type (with double CPU) giving consideration to that of the model HR-S9500U by way of example.

3.1.1 Outline of syscon system

Fig. 3-1-1 shows a block diagram of serial bus line connection of the HR-S9500U's syscon system.
This syscon system is composed of two IC chips: one is IC3001 that serves as the main CPU in the master side and the other is IC3301 that serves as the sub CPU in the slave side.
The main routine program for the whole syscon system is written in the IC3001 of the main CPU.
The IC3001 of the main CPU fundamentally controls the circuits of the timer system, on-screen system and tuner system besides the IC3301 of the sub CPU.
The IC3301 that serves as the sub CPU in the slave side as mentioned above fundamentally controls the circuits of the mechanism system, servo system, video system and audio system. The IC3301 directly controls the above-mentioned circuits according to the control program incorporated inside, however, its function is just like an expander.
Those two IC's communicate to each other through the 8-bit serial and parallel bus lines between the pins 34 to 41 of the IC3301 and the pins 31 to 38 of the IC3001.

3.1.2 Outline of doctor system

Compared with models for the years before 1998, there is another important change in the syscon system of 1998 VTR models having a couple of CPU's.
As noticed in our Service Bulletin, the syscon system of such the previous models needs resetting (disconnecting/connecting resistors, etc.) each time the CPU or EEPROM for the syscon system is replaced. If the syscon system is not reset after replacement of the CPU or EEPROM, the syscon system occasionally fall into the hang-up status.
Regarding the syscon system of 1998 models that incorporate HITACHI microcomputers (IC's whose part numbers are respectively led by HD such as HDxxxx) for the syscon system, the data on its version is written in the EEPROM for the syscon system. Furthermore, the system to recognize the version of the service EEPROM is incorporated in the CPU. Therefore, the syscon system incorporating a HITACHI microcomputer has no need of resetting (disconnecting/connecting resistors, etc.) after replacement of the CPU or EEPROM for the syscon system.
However, the syscon system of some 1998 VTR models incorporating a couple of CPU's employs MITSUBISHI micro computers (IC's whose part numbers are led by M such as Mxxxx). Note that this syscon system (employing MITSUBISHI microcomputers) needs resetting (disconnecting/connecting resistors, etc.) after replacement of the CPU or EEPROM for the syscon system.

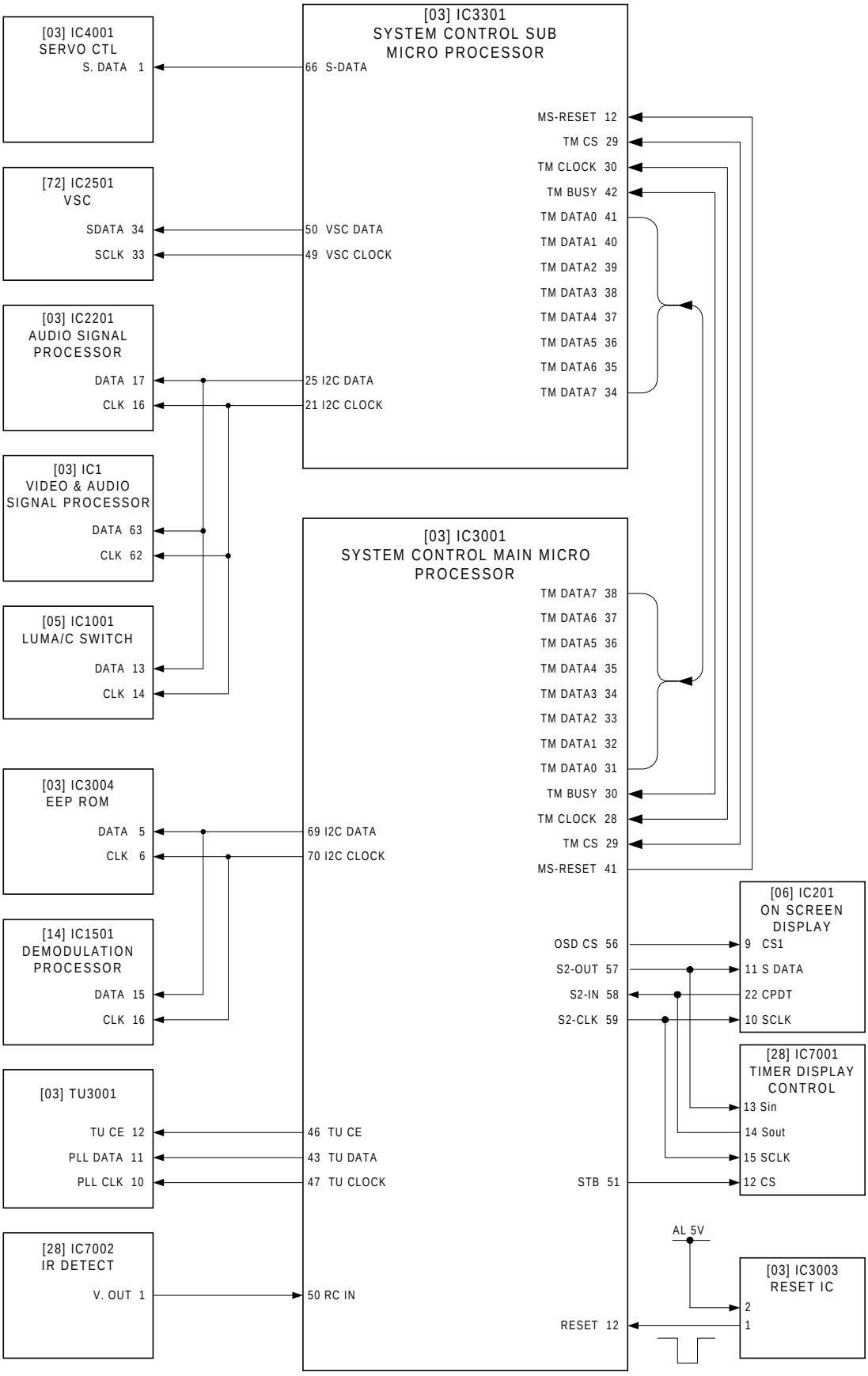

Fig. 3-1-1 Syscon block diagram

SECTION 4
SERVO CIRCUIT

4.1 EXPLANATION OF SERVO CIRCUIT

The servo circuit of all JVC models except the DD and S-VHS models of the year of 1998 adopts the software servo system which is incorporated in the syscon CPU, while the servo circuit of the DD and S-VHS models adopts the digital servo system that has the independent servo IC as same as the past models.

Since there is nothing new to report particularly in the digital servo system of the 1998 models, the following gives explanation of the software servo system of the model HR-A34U by way of example.

4.2 SIGNAL PROCESSING IN RECORDING

Fig. 4-2-1 shows the servo signal flow in recording.

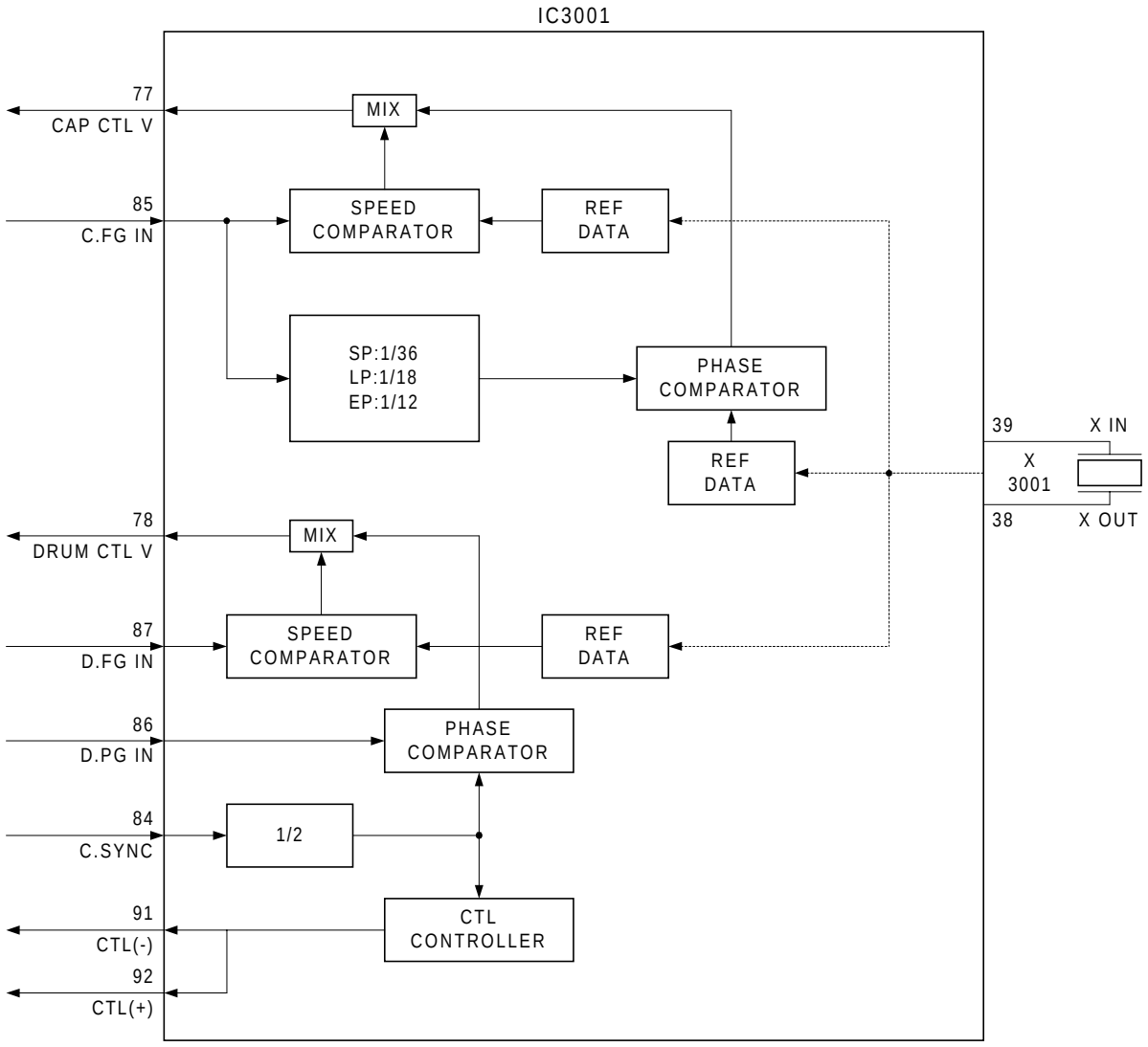

Fig. 4-2-1 Servo signal flow in recording.

4.2.1 Processing of DRUM SERVO signal

The DRUM FG IN signal (input to pin 87) and DRUM PG IN signal (input to pin 86) are used to control the drum servo system.

Error in the speed control system is obtained by the SPEED COMPARATOR circuit, which compares the actual period of the DRUM FG signal with the theoretical period of the DRUM FG that the reference clock of X301 is counted with REF DATA. The REF DATA of the speed control system is fixed.

Error in the phase control system is obtained by the PHASE COMPARATOR circuit, which compares the actual timing of the DRUM PG signal with the timing of a half-divided frequency (1/2 H. SYNC = frame frequency) of H. SYNC that is extracted from C. SYNC signal of video signal.

The above-mentioned two errors are processed by the MIX circuit to be mixed as a resultant error, and the MIX circuit controls the DRUM CTL V signal (output from pin 78) so as to eliminate the resultant error.

4.2.2 Processing of CAPSTAN SERVO signal

The CAP FG signal (input to pin 85) is used to control the capstan servo system.

Error in the speed control system is obtained by the SPEED COMPARATOR circuit, which compares the actual period of the CAPSTAN FG signal with the theoretical period of the CAPSTAN FG that the reference clock of X301 is counted with REF DATA. The REF DATA of the speed control system varies depending on the tape speed mode.

Error in the phase control system is obtained by the PHASE COMPARATOR circuit, which compares the actual timing of a divided frequency (frame frequency) of the CAPSTAN FG signal with the theoretical timing of the frame frequency that the reference clock of X301 is counted with the REF DATA.

The capstan of the HR-A34U generates 360 FG pulses per rotation. The rotation speed of the capstan is 3 Hz in the SP mode, 1.5 Hz in the LP mode, or 1 Hz in the EP mode.

Therefore, the timing of the frame frequency is decided by dividing the FG into 1/36 for the SP mode, 1/18 for the LP mode or 1/12 for the EP mode.

The REF DATA of the phase control system is fixed.

The above-mentioned two errors are processed by the MIX circuit to be mixed as a resultant error, and the MIX circuit controls the CAP CTL V signal so as to eliminate the resultant error.

The control pulses (outputs from pins 91 and 92) are generated timing with a half-divided frequency (frame frequency) of H. SYNC signal that is extracted from the C. SYNC signal.

4.3 SIGNAL PROCESSING IN PLAYBACK

Fig. 4-3-1 shows the servo signal flow in playback.

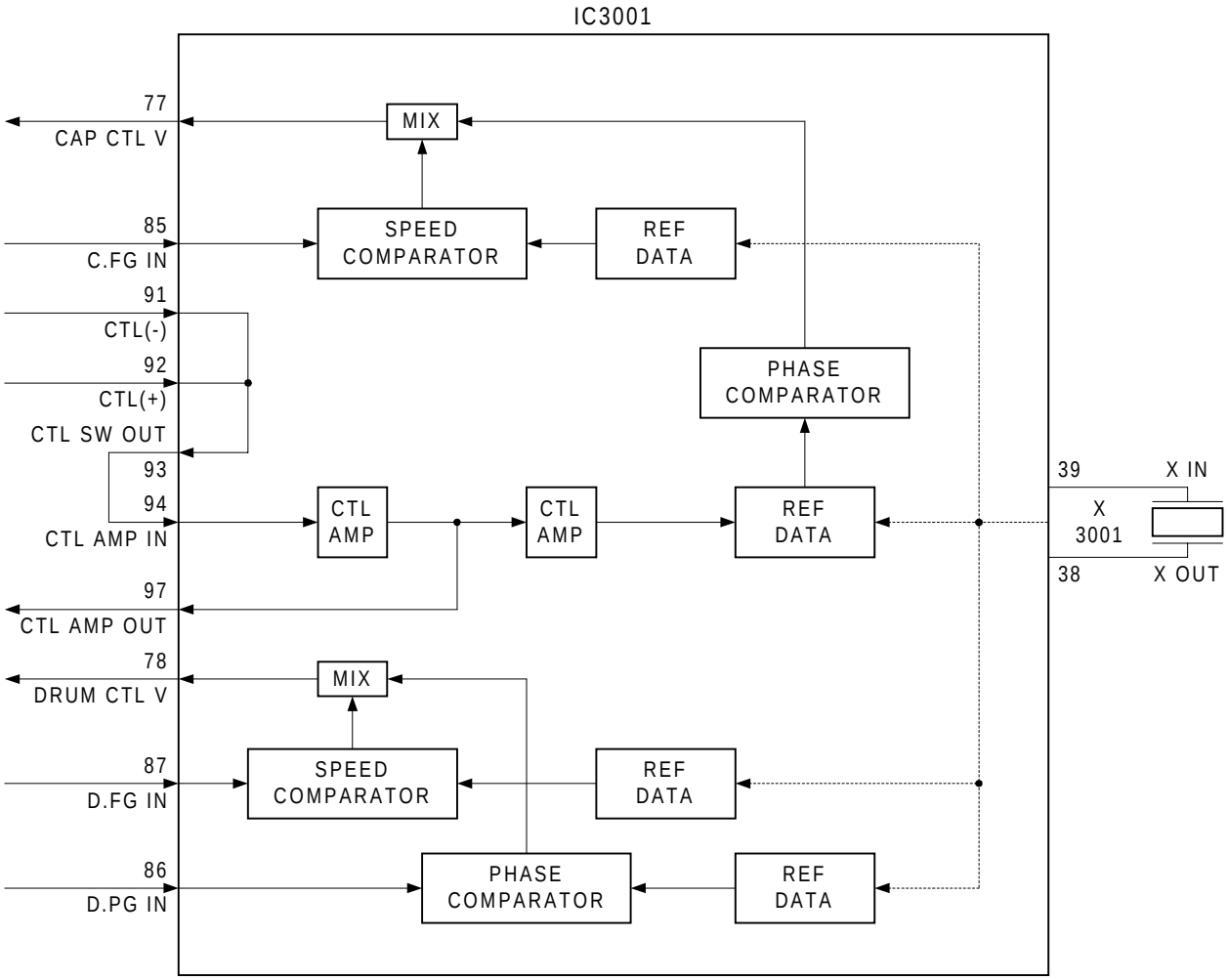

Fig. 4-3-1 Servo signal flow in playback.

4.3.1 Processing of DRUM SERVO signal

The DRUM FG IN signal (input to pin 87) and DRUM PG IN signal (input to pin 86) are used to control the drum servo system.

Error in the speed control system is obtained by the SPEED COMPARATOR circuit, which compares the actual period of the DRUM FG signal with the theoretical period of the DRUM FG that the reference clock of X301 is counted with REF DATA. The REF DATA of the speed control system varies depending on the playback tape speed (fH correction).

Error in the phase control system is obtained by the PHASE COMPARATOR circuit, which compares the actual period of the DRUM PG with the theoretical period of the DRUM PG that the reference clock is counted with the REF DATA.

The REF DATA of the phase control system varies depending on the playback tape speed (fH correction).

The above-mentioned two errors are processed by the MIX circuit to be mixed as a resultant error, and the MIX circuit controls the DRUM CTL V signal (output from pin 78) so as to eliminate the resultant error.

4.3.2 Processing of CAPSTAN SERVO signal

The CAP FG signal (input to pin 85) and the control pulses (input to pins 91 and 92) are used to control the capstan servo.

Error in the speed control system is obtained by the SPEED COMPARATOR circuit, which compares the actual period of the CAPSTAN FG signal with the theoretical period of the CAPSTAN FG that the reference clock of X301 is counted with REF DATA. The REF DATA of the speed control system varies depending on the tape speed mode.

Error in the phase control system is obtained by the PHASE COMPARATOR circuit, which compares the control pulses with the theoretical timing of the frequency that the reference clock of X301 is counted with the REF DATA.

The REF DATA of the phase control system varies depending on the playback tape speed.

SECTION 5
EXPLANATION OF TYPE 29 MECHANISM

5.1 OUTLINE

The type 29 mechanism is an improved version of the type 22 mechanism and it is developed under the design conception aiming at high serviceability, high response performance and down-sizing for saving space. The type 29 mechanism is composed of more simplified parts as compared with the type 22 mechanism. The cassette housing operation are described below.

5.2 MECHANISM MODES AND FUNDAMENTAL OPERATION

5.2.1 Operation of cassette housing

1) Flowchart of cassette intake operation

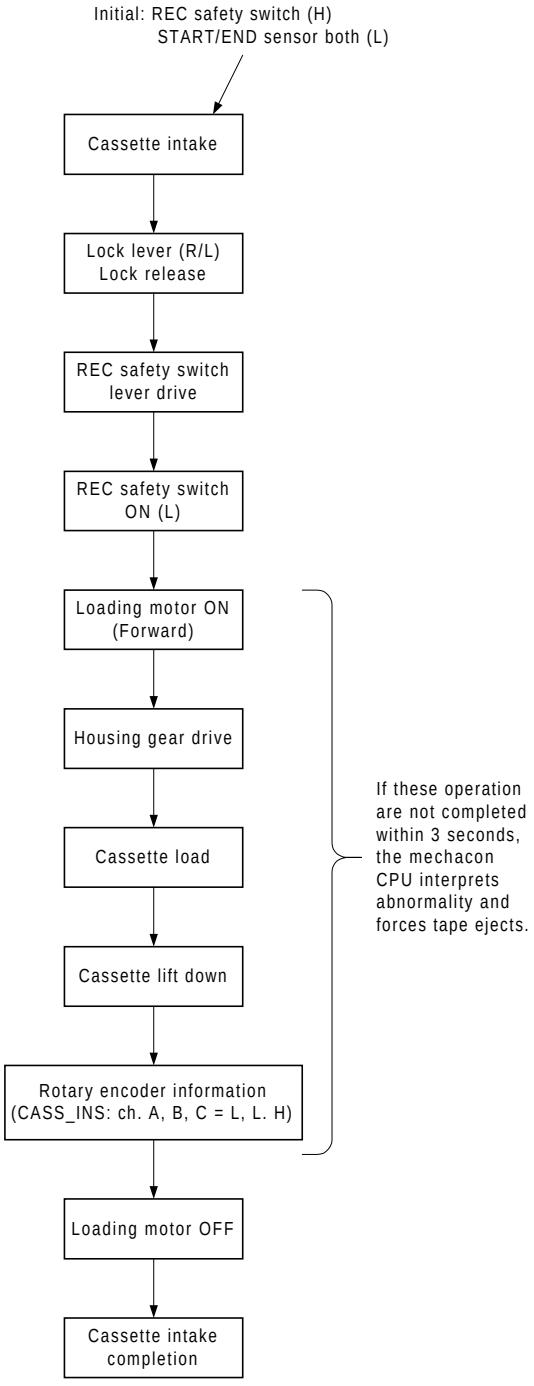

Fig. 5-2-1 Flowchart of cassette intake operation

2) Flowchart of cassette eject operation

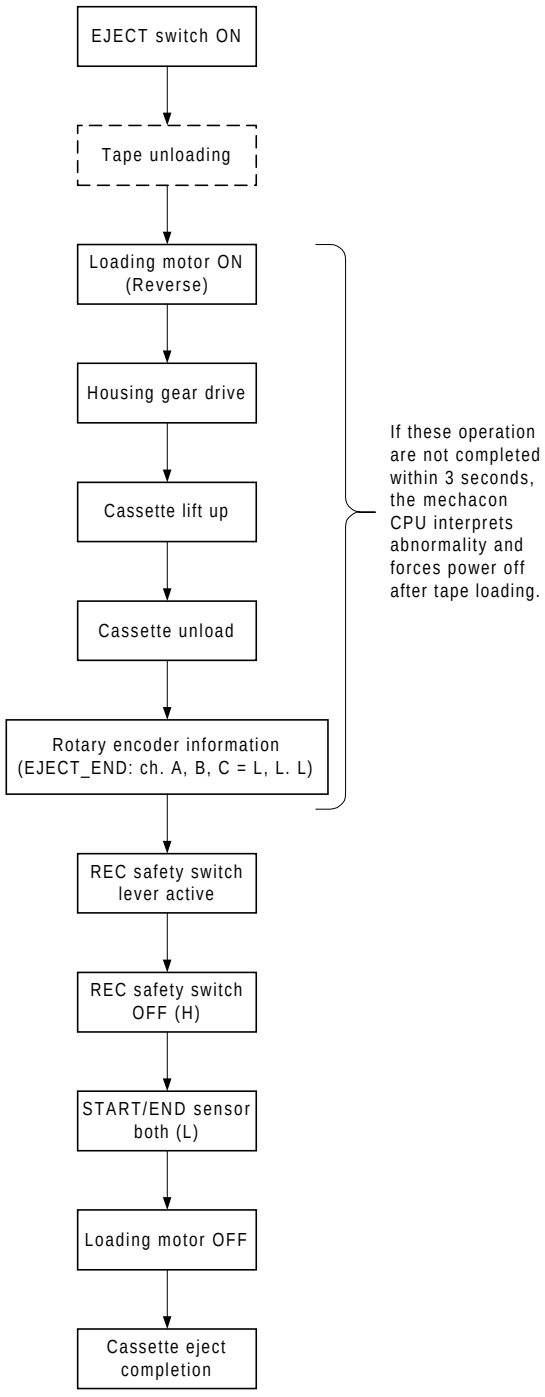

Fig. 5-2-2 Flowchart of cassette eject operation

3) Switch status and sensor status

Cassette housing status	REC safety switch output	Start sensor output	End sensor output
Cassette absent	H	L	L
During cassette intake	L	L	L
Cassette intake complete	H/L	H	H
During cassette eject	L	L	L
Cassette eject complete	H	L	L

Table 5-2-1 Relation between switch and sensor outputs and cassette housing status

The REC SAFETY switch is also used to detect insertion of a video cassette, and the double function of the REC SAFETY switched by the SYSCON CPU according to mode information from the rotary encoder. When the mechanism is in the status between the EJECT END mode and the CASS-UP mode, the REC SAFETY switch serves as the cassette insertion detector switch. If a video cassette is inserted in the EJECT END mode, the REC SAFETY switch outputs an "H" level signal to the SYSCON CPU to inform it that a video cassette is inserted, and the mechanism accordingly starts cassette intake operation.
After the CASS-INS mode, or after completion of cassette intake operation in other words, the REC SAFETY switch does its original duty as the recording safety switch. After cassette intake operation is complete, if the REC SAFETY switch outputs an "L" level signal, the SYSCON CPU recognizes that a video cassette without a recording protection tab is inserted and is commands the mechanism to start automatic playback operation.
If outputs of both the START sensor and END sensor are "L" level after completion of cassette intake operation, the SYSCON CPU recognizes that the cassette tape is broken and the mechanism automatically starts tape eject operation under a command of the SYSCON CPU.

5.2.2 Mechanism mode shift diagram

For operation timing of main mechanism parts in each mechanism mode, refer to the following mechanism mode shift diagram.

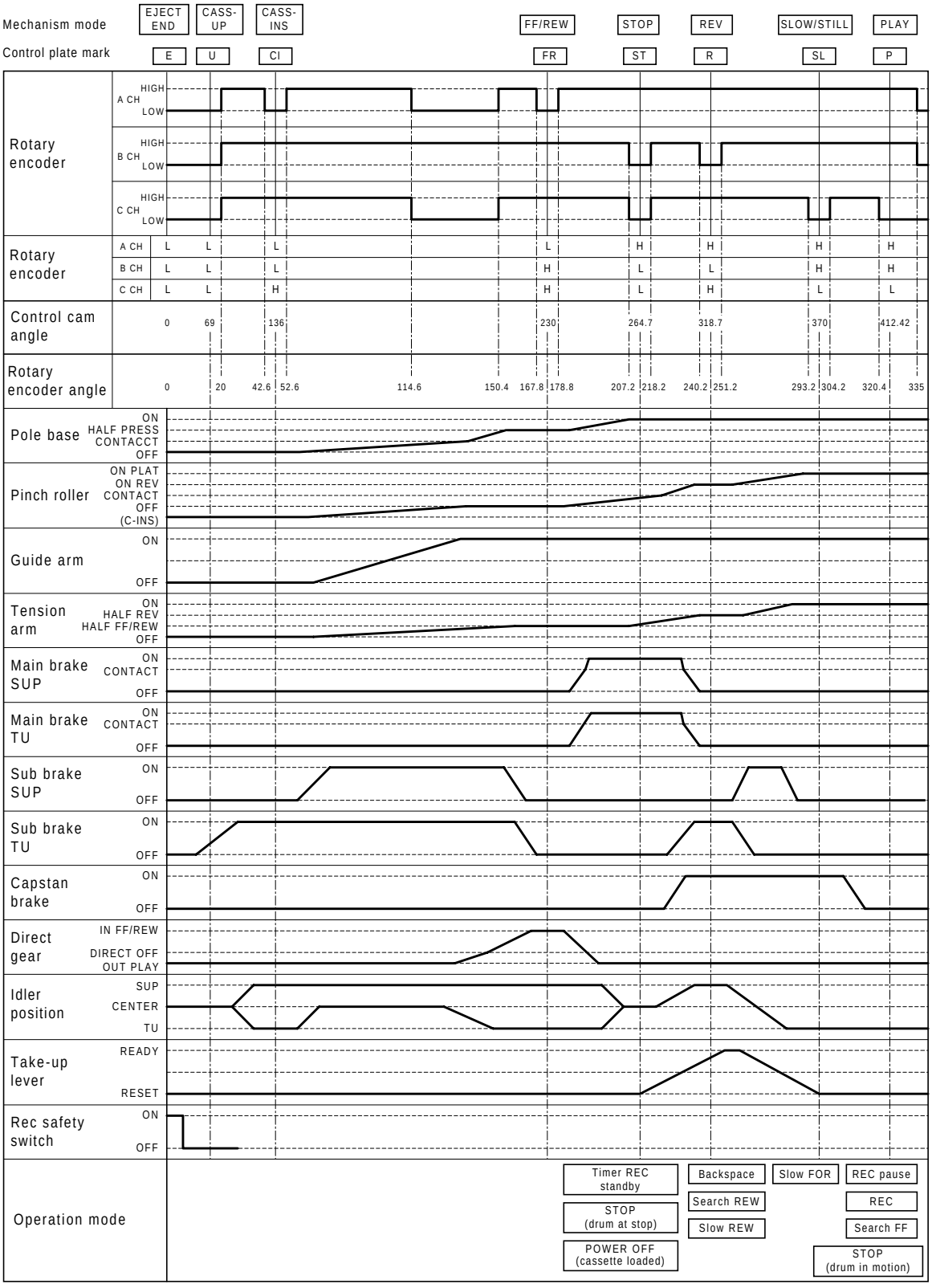

Table 5-2-2 Mechanism mode shift diagram

5.3 OPERATION OF MECHANISM PARTS

Each mechanism part performs operation under control of the control cam and control plate. The control cam turns by the loading motor's drive power that is transmitted through the worm gear. Rotation of the control cam is transmitted to the control plate through the link lever assembly. Operations of the control cam and control plate are monitored by the rotary encoder that is combined with the control plate, and monitor results are transmitted to the SYSCON CPU.

Mechanism operation will be illustrated in the following with a flowchart that divides mechanism operation into some blocks and some figures of the control cam and control plate.

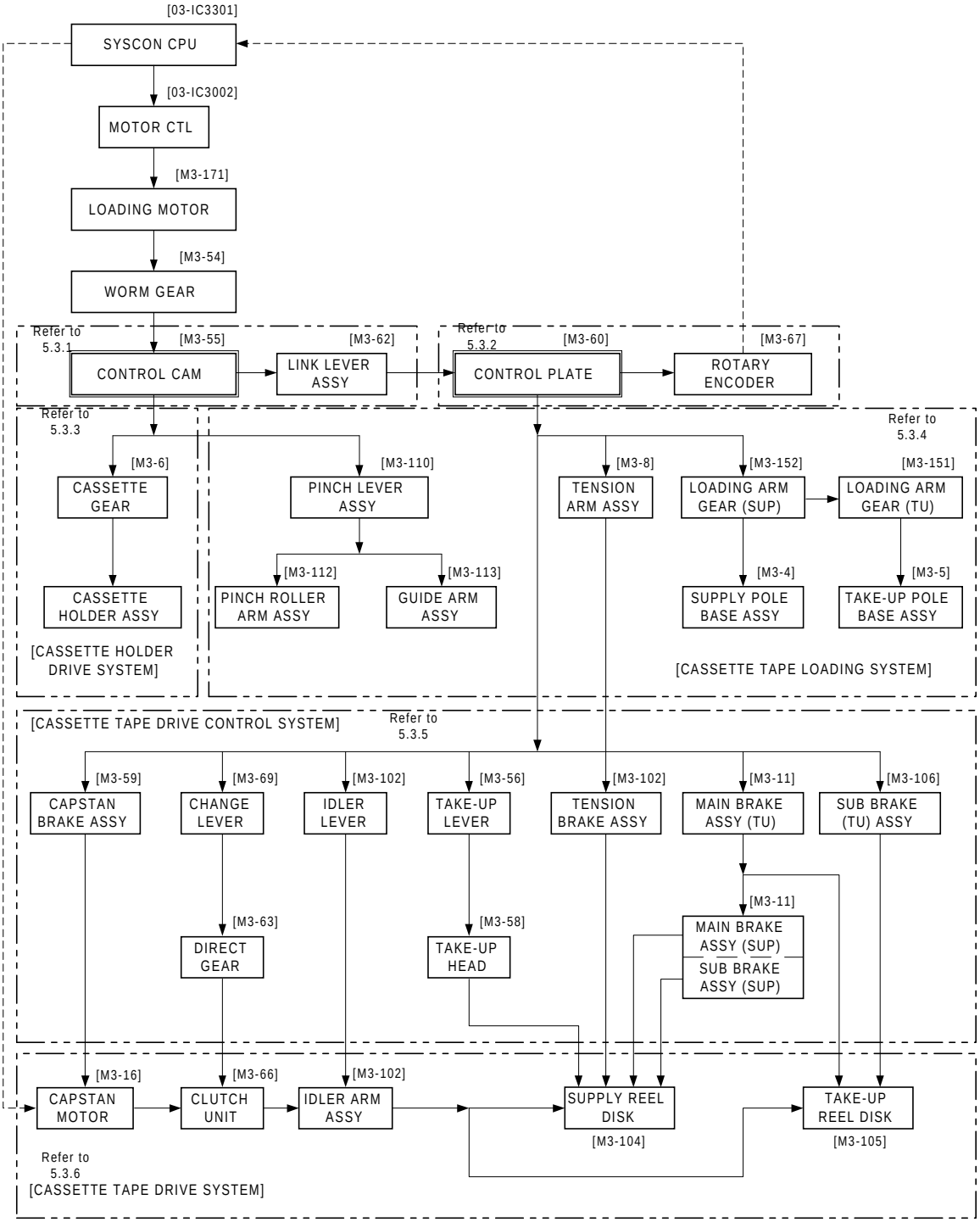

Fig. 5-3-1 Mechanism operation flowchart

5.3.1 Component parts controlled by control cam

The control cam controls the cassette gear and pinch lever assembly, and it also controls the control plate through the link lever assembly as shown in Fig. 5-3-1.
Since the above-mentioned parts are engaged with the control cam by their respective gear teeth, trace pin and so on, those parts start their workings with rotation of the control cam. The shape of the control cam is outlined in Fig. 5-3-2 and 5-3-3.

Fig. 5-3-2 Control cam
(View from the lower side of the mechanism chassis)

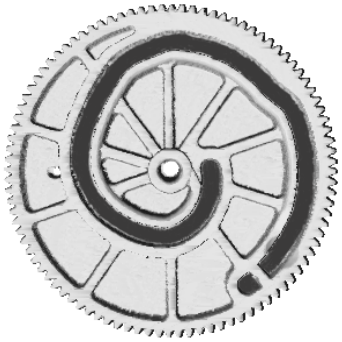

Fig. 5-3-3 Control cam
(View from the upper side of the mechanism chassis)

1) Link lever assembly

The link lever assembly drives the control plate.
The link lever assembly is engaged with the control cam by the control cam's groove shown in Fig. 5-3-4 (control cam viewed from the lower side of the mechanism chassis) and the trace pin of the link lever assembly.
Movement of the trace pin is controlled by the shape of the control cam's groove, therefore, the link lever assembly converts rotational movement into sidewise movement according to change of the linear travel distance between the center of the control cam and the trace pin, and the control plate is resultingly driven by the link lever assembly.

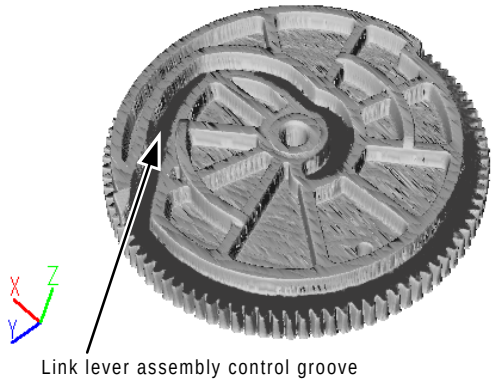

Fig. 5-3-4 Control cam (Link lever assembly drive part)

5.3.2 Component parts controlled by control plate

The control plate is engaged with the link lever assembly by the lock pin (shown in Fig. 5-3-5) of the former and the control hole of the latter. Rotational movement of the control cam is converted into sidewise movement by the link lever assembly, therefore, the control plate is driven sideways by the link lever assembly.

The control plate not only controls the tension arm assembly, loading arm gear (SUP), capstan brake, change lever, idler lever, take-up lever, main brake assembly (TU) and sub brake assembly (TU), but also drives the rotary encoder in order to correctly convey the operation status of the mechanism to the SYSCON CPU.

The above-mentioned parts are connected with the control plate by their respective gear teeth, trace pin and so on, therefore, those parts are operated by sidewise movement of the control plate. The shape of the control plate is shown in Fig. 5-3-5 and 5-3-6.

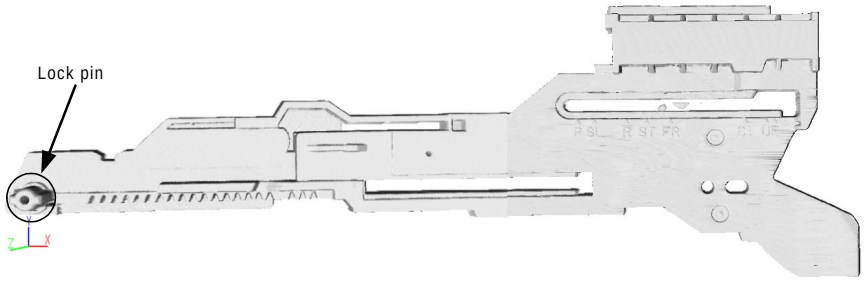

Fig. 5-3-5 Control plate (View from the lower side of the mechanism chassis)

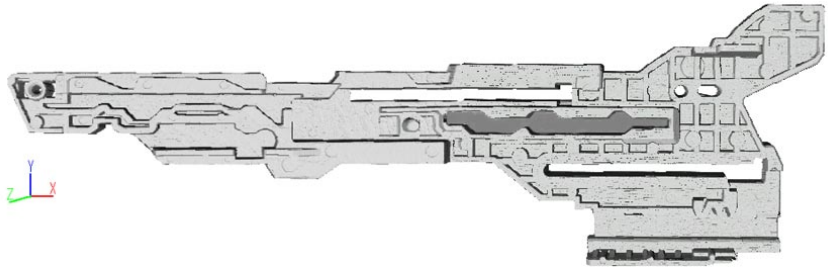

Fig. 5-3-6 Control plate (View from the upper side of the mechanism chassis)

1) Rotary encoder

The rotary encoder is assembled in the mechanism taking a good phase in the mechanism assembly mode, and it correctly conveys the status of the mechanism mode to the SYSCON CPU when the control plate takes movement.

The rotary encoder is connected with the gear of the control plate shown in Fig. 5-3-7 (control plate viewed from the lower side of the mechanism chassis).

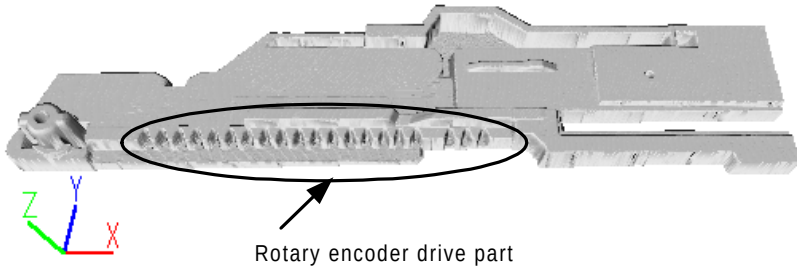

Fig. 5-3-7 Control plate (Rotary encoder drive part)

5.3.3 Cassette holder drive system

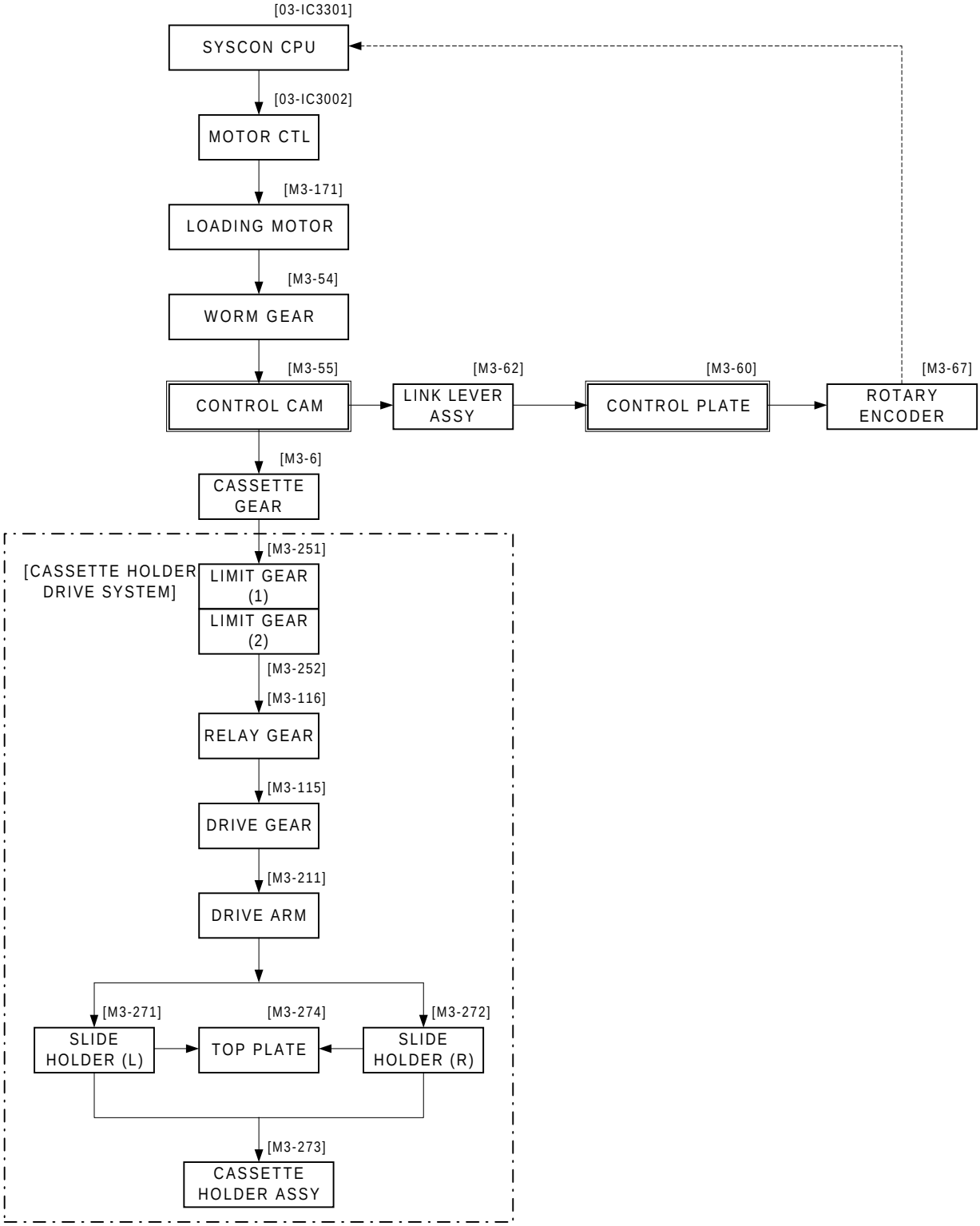

Fig. 5-3-8 Cassette holder drive system flowchart

1) Cassette gear [M3-6]
The cassette gear drives the cassette holder assembly.
The cassette gear is engaged with the circumferential gear of the control cam. See the figure below (Fig. 5-3-9) that shows the control cam as viewed from the lower side of the mechanism chassis.

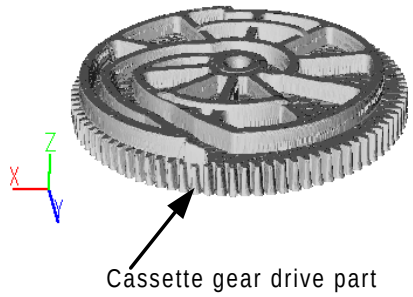

Fig. 5-3-9 Control cam (Cassette gear drive part)

5.3.4 Cassette tape loading system

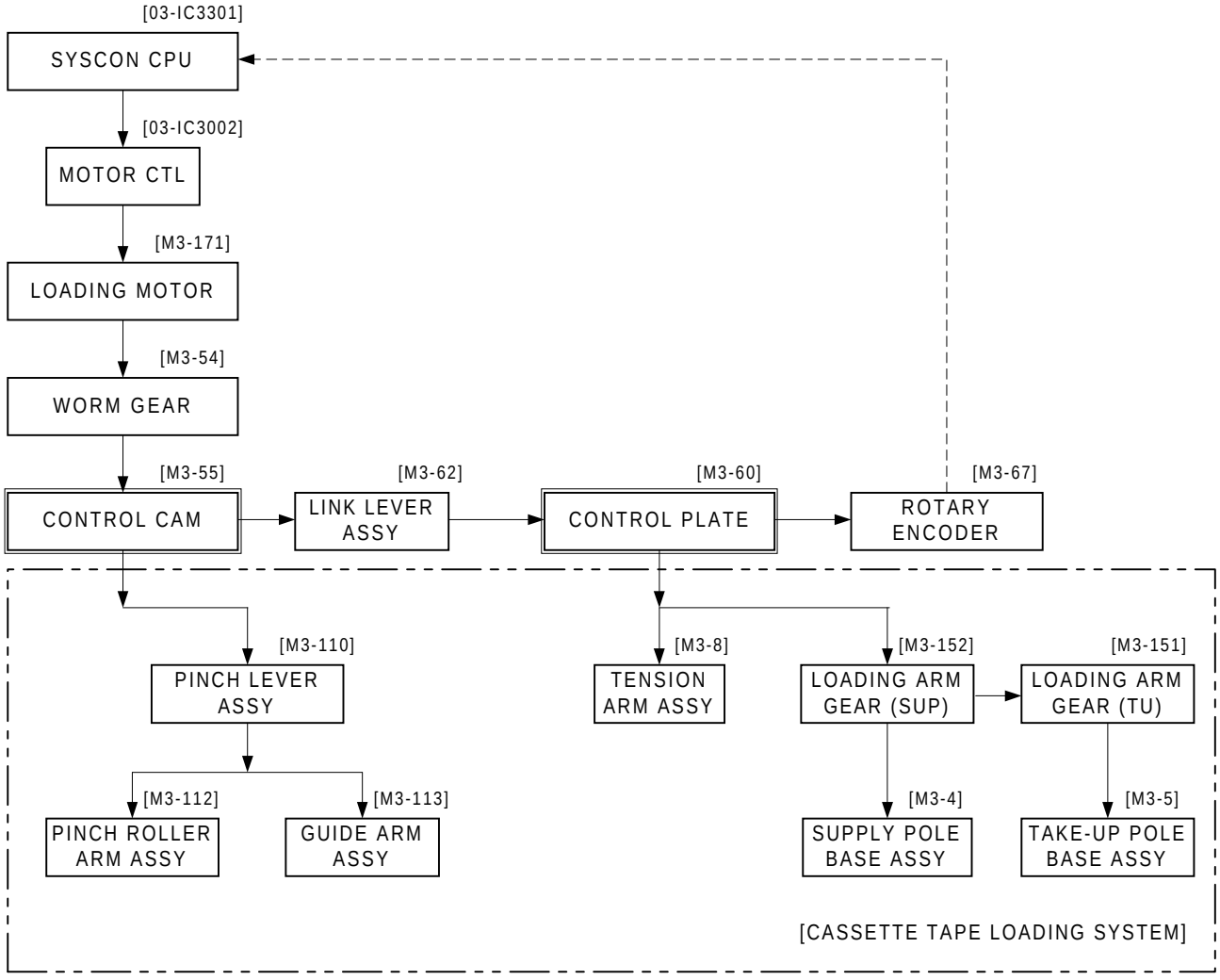

Fig. 5-3-10 Flowchart of cassette tape loading system

1) Pinch lever assembly [M3-110]

The pinch lever assembly not only drives the pinch roller arm assembly and guide arm assembly but controls the cassette tape loading system (TU side).

The pinch lever assembly is connected with the control cam by its trace pin that is set in the groove on the control cam. (See Fig. 5-3-11 that shows the control cam as viewed from the upper side of the mechanism chassis.)

Since the trace pin of the pinch lever assembly is controlled by the shape of the groove on the control cam, the pinch lever assembly drives the pinch roller arm assembly and guide arm assembly by converting rotational movement of the control cam into sidewise movement according to change of the linear movement distance from the center of the control cam to the trace pin.

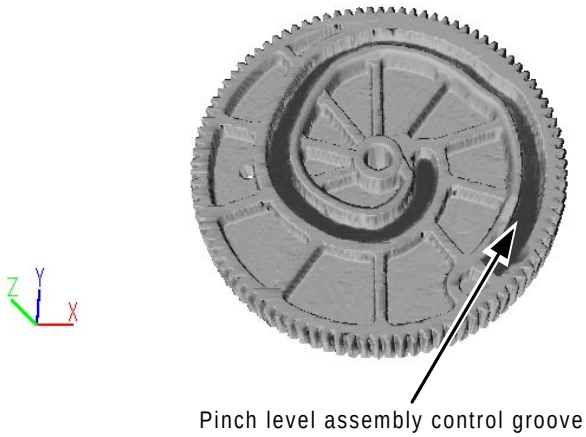

Fig. 5-3-11 Control cam (Pinch lever assembly drive part)

2) Tension arm assembly [M3-8]

The tension arm assembly serves not only to control the cassette tape loading system (SUP side) but to drive the tension brake assembly.

Since the trace pin of the tension arm assembly contacts the edge part of the control plate (see Fig. 5-3-12 that shows the control plate as viewed from the lower side of the mechanism chassis), the tension arm assembly works with movement of the control plate. When the trace pin of the tension arm assembly travels from the part (a) to the part (b) (appearing in Fig. 5-3-12) of the control plate as the control plate moves sideways, the tension arm assembly starts cassette tape loading operation.

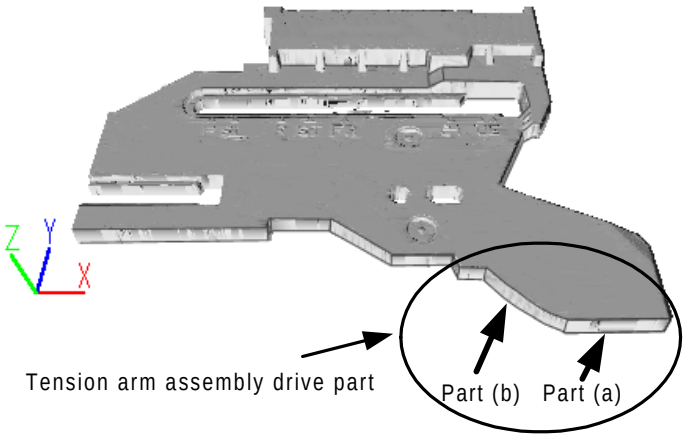

Fig. 5-3-12 Control plate (Tension arm assembly drive part)

3) Loading arm gear (SUP) [M3-152]

While the loading arm gear (SUP side) controls the cassette tape loading system of the SUP side by driving the supply pole base assembly, it also controls the cassette tape loading system of the TU side by driving the take-up pole base assembly through the loading arm gear (TU side).

The loading arm gear (SUP side) is engaged with the gear of the control plate, which appears in Fig. 5-3-13 that shows the control plate as viewed from the upper side of the mechanism chassis.

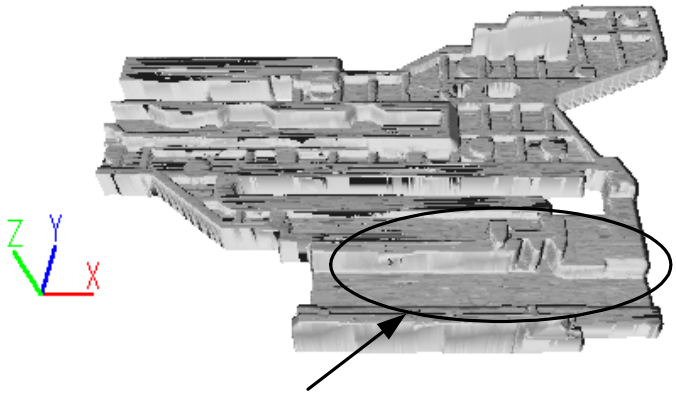

Fig. 5-3-13 Control plate (Loading arm gear drive part)

5.3.5 Cassette tape drive control system

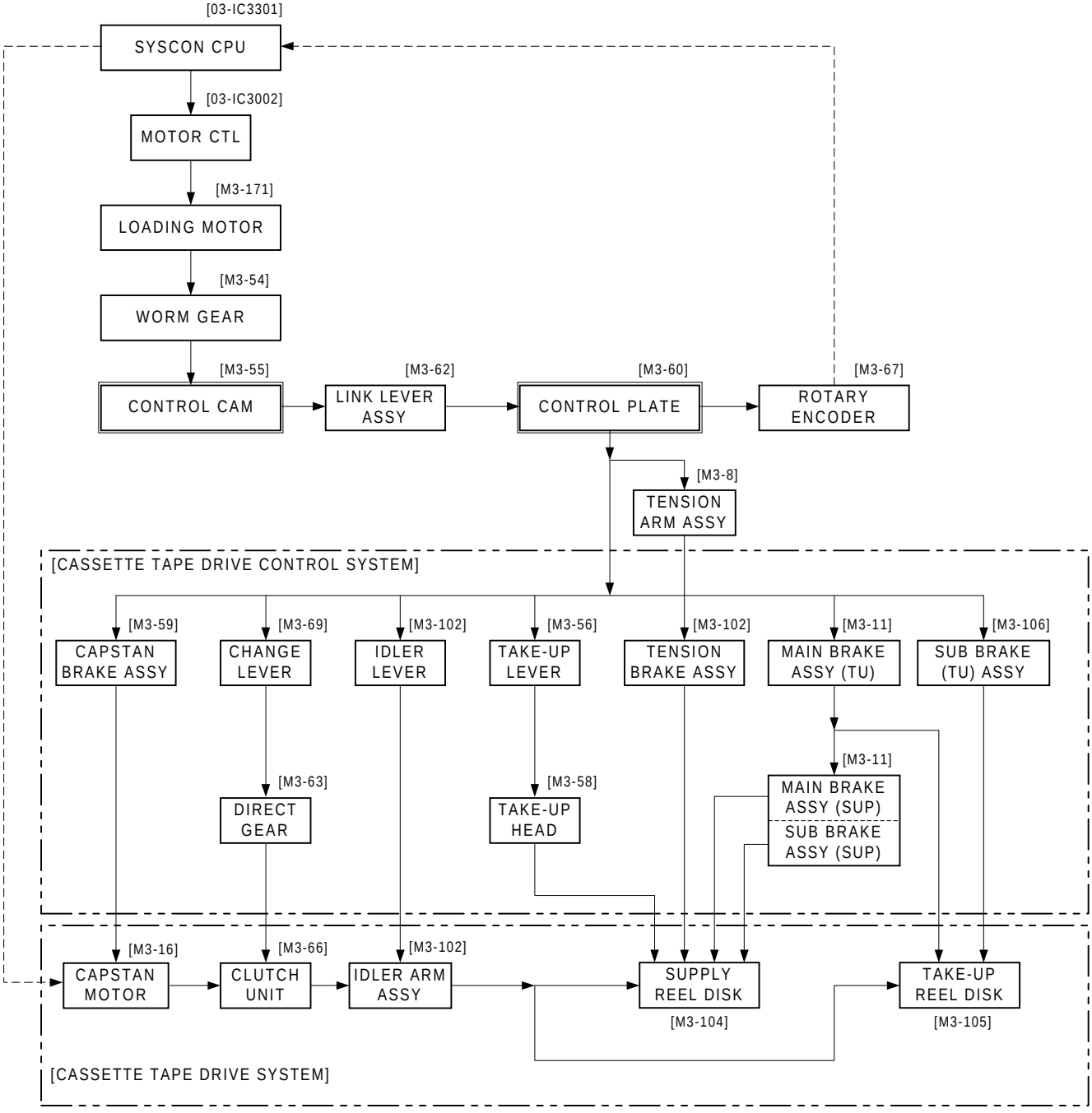

Fig. 5-3-14 Cassette tape drive control system flow

1) Capstan brake assembly [M3-59]

The capstan brake assembly applies the brakes on the capstan motor.

The capstan brake assembly is set so that its arm contacts the edge part of the control plate, which appears in Fig. 5-3-15 that shows the control plate as viewed from the lower side of the mechanism chassis. When the arm of the capstan brake assembly is located at the part (c) of the control plate, the capstan brake assembly is out of braking work. However, when the arm comes into contact with the part (d) of the control plate, the capstan brake assembly puts the brake on the capstan because the arm is pushed out by the part (d).

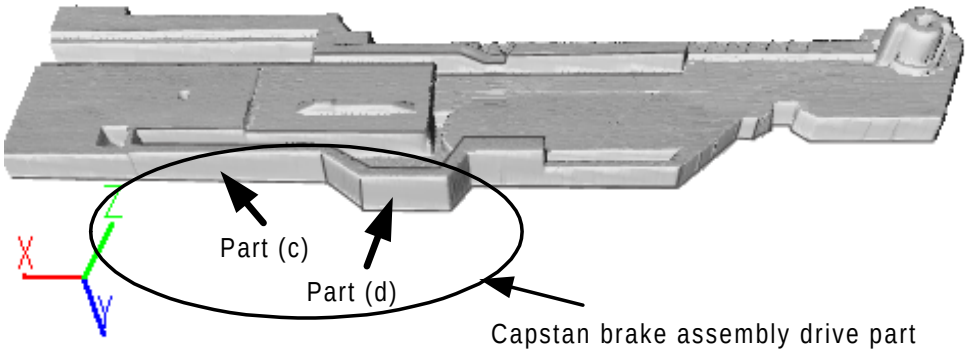

Fig. 5-3-15 Control plate (Capstan brake assembly drive part)

2) Change lever [M3-69]

The change lever assembly drives the direct gear and accordingly controls the clutch unit.

Since the change lever is constructed so as to work in seesaw motion, it controls the direct gear according to movement of the control plate.

The change lever assembly is set so that its arm usually contacts a crest part of the control plate (see Fig. 5-3-16 that shows the control plate as viewed from the lower side of the mechanism chassis) while it presses the direct gear down by the other part in the opposite side. The direct gear is always pushed up by the built-in spring.

Resultingly, the change lever presses the direct gear down when its arm is located in the crest part of the control plate, however, the direct gear is pushed up by the internal spring when the arm of the change lever is located in the trough part where the arm is free from duty.

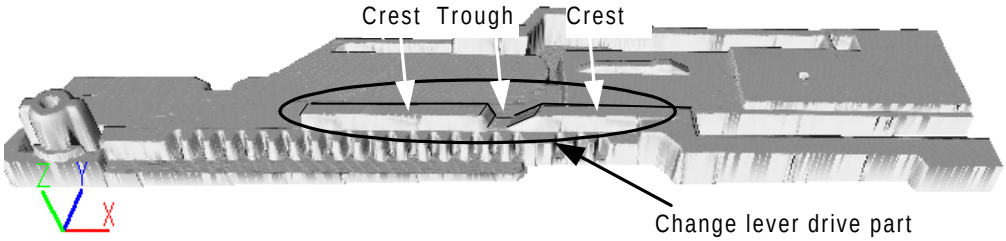

Fig. 5-3-16 Control plate (Change lever drive part)

3) Idler lever [M3-102]

The idler lever forcibly controls the working direction of the idler arm assembly depending on the mechanism mode.

The idler lever is connected with the control plate by its trace pin, which is set in the control groove on the control plate (see Fig. 5-3-17 that shows the control plate as viewed from the upper side of the mechanism chassis).

Since movement of the trace pin of the idler lever is controlled by the varied shape of the groove on the control plate, the idler lever controls working direction of the idler arm assembly so as to move it towards the supply reek disk drive side or the take-up reel disk drive side or to stop it at the center position.

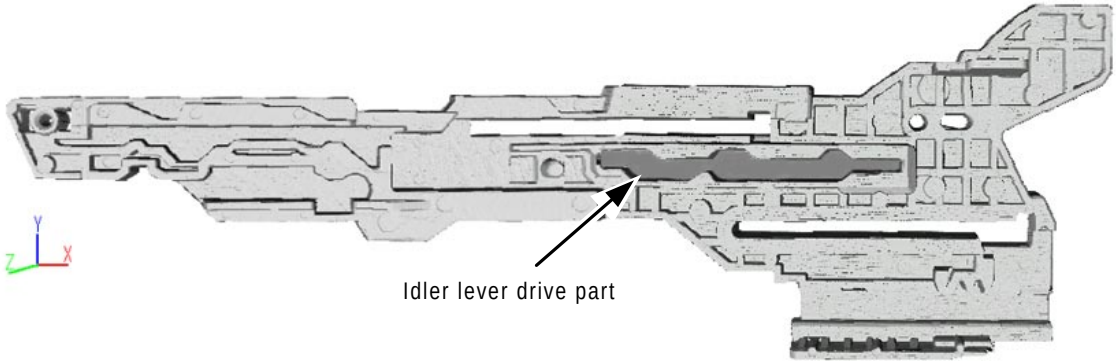

Fig. 5-3-17 Control plate (Idler lever drive part)

4) Take-up lever [M3-56]

The take-up lever applies the brakes on the supply reel disk through the take-up head.

The take-up lever is connected with the control plate by its trace pin, which contacts the edge part of the control plate (see Fig. 5-3-18 that shows the control plate as viewed from the upper side of the mechanism chassis). The take-up lever is always pulled by the tension spring in the direction to apply the brakes on the supply reel disk, however, its operation is controlled by the control plate.

When the trace pin of the take-up lever is located between the part (e) and part (f) of the control plate, the take-up lever is released from control of the control plate and it accordingly drives the take-up head to put the brake on the supply reel disk.

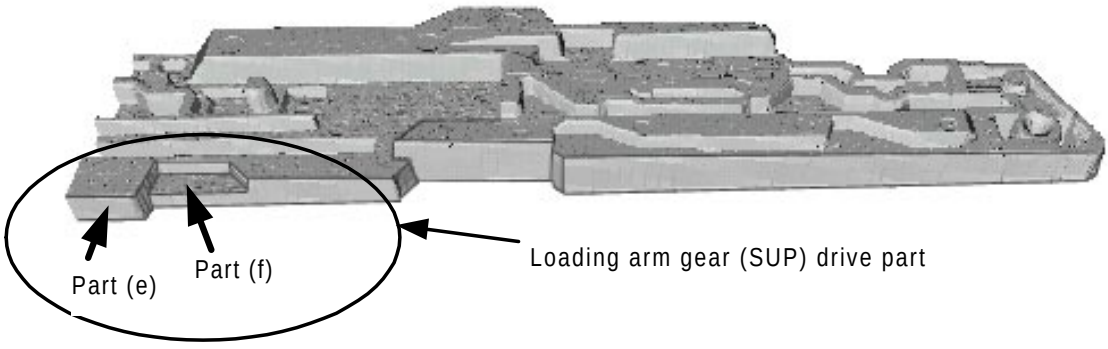

Fig. 5-3-18 Control plate (Take-up lever drive part)

5) Tension brake assembly [M3-102]

The tension brake assembly that is driven by the tension arm assembly applies the brakes on the supply reel disk.

When the trace pin of the tension brake assembly is located at the edge part (b) of the control plate (see Fig. 5-3-19 that shows the control plate as viewed from the lower side of the mechanism chassis), the tension brake assembly puts the brake on the supply reel disk.

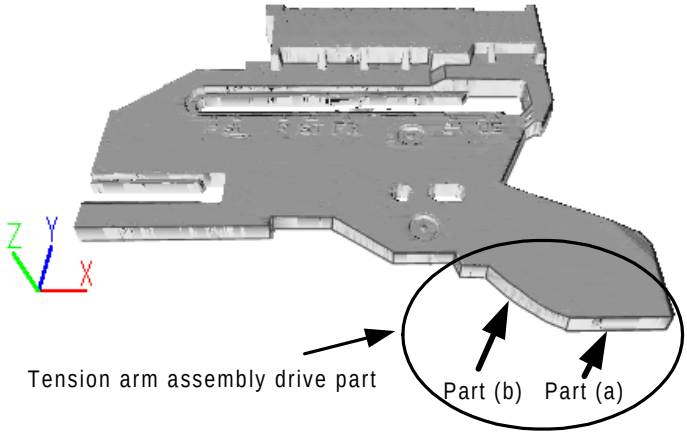

Fig. 5-3-19 Control plate (Tension arm assembly drive part)

6) Main brake assembly (TU) [M3-11]

The main brake assembly (TU) not only applies the brakes on the take-up reel disk depending on the mechanism mode but also does the same on the supply reel disk by driving the main brake assembly (SUP)/sub brake assembly (SUP).

The main brake assembly (TU) is connected with the control plate by its trace pin that is set in the control groove on the control plate (see Fig. 5-3-20 that shows the control plate as viewed from the upper side of the mechanism chassis).

Since movement of the trace pin of the main brake assembly (TU) is controlled by the varied shape of the control groove on the control plate, the main brake assembly puts the brake on the take-up reel disk and supply reel disk depending on the mechanism mode.

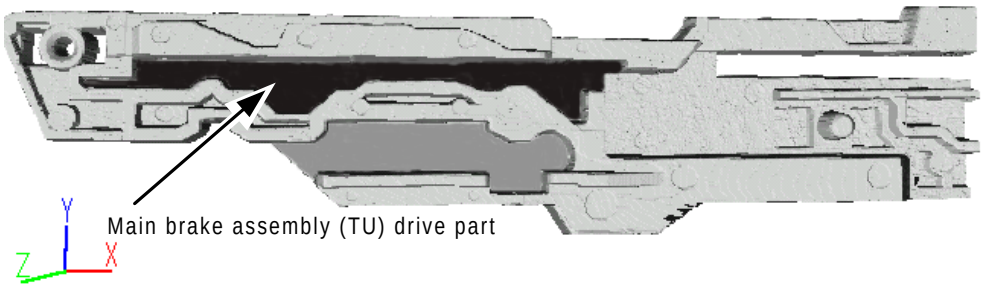

Fig. 5-3-20 Control plate (Main brake assembly drive part)

7) Sub brake (TU) assembly [M3-106]

The sub brake (TU) assembly applies the brakes on the take-up reel disk depending on the mechanism mode.

The sub brake (TU) assembly is connected with the control plate by its trace pin that is set in the control groove on the control plate (see Fig. 5-3-21 that shows the control plate as viewed from the upper side of the mechanism chassis).

Since movement of the trace pin of the sub brake (TU) assembly is controlled by the varied shape of the control groove on the control plate, the sub brake assembly puts the brake on the take-up reel disk depending on the mechanism mode.

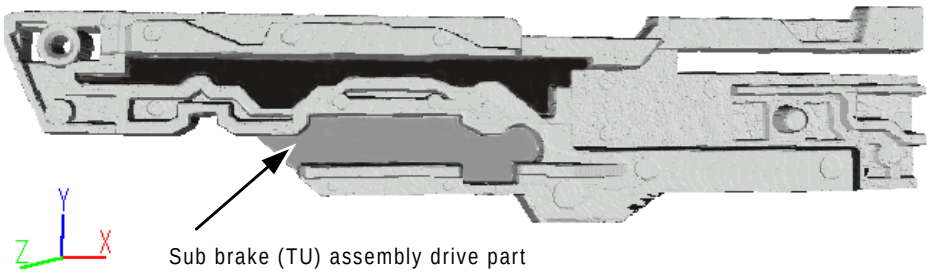

Fig. 5-3-21 Control plate (Sub brake [TU] ass'y drive part)

5.3.6 Cassette tape drive system

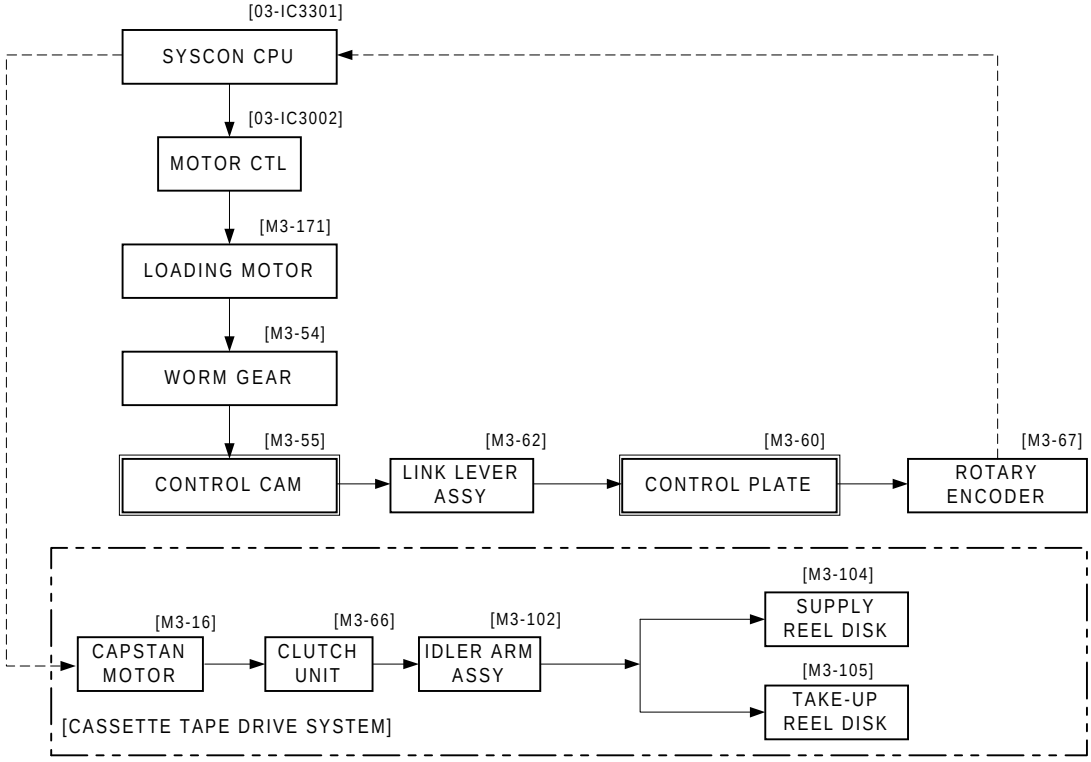

Fig. 5-3-22 Flowchart of cassette tape drive system

1) Capstan motor [M3-16]
The capstan motor drives the supply reel disk and take-up reel disk through the clutch unit and idler arm assembly as shown in Fig. 5-3-22.
Operation of the capstan motor is controlled by the SYSCON CPU depending on the mechanism mode.

2) Clutch unit [M3-66]
The clutch unit functions to adjust the driving force of the capstan motor while transmitting it to the idler arm assembly.
Since operation of the clutch unit is controlled by the direct gear depending on the mechanism mode, it transmits the driving force of the capstan motor to the supply reel disk or take-up reel disk without attenuation of the driving force in the FF/REV mode. In the other modes the clutch unit transmits the driving force of the capstan motor to the idler arm assembly after it attenuates the driving force to a degree that the cassette tape and the tape transport system are not burdened with it.

3) Idler arm assembly [M3-102]
The idler arm assembly functions to transmit the driving force of the capstan motor to the supply reel disk or take-up reel disk.
On the other hand, the idler arm assembly functions to cut off the driving force of the capstan motor not to be transmitted to the supply reel disk or take-up reel disk in some mechanism modes, because operation of the idler arm assembly is controlled by the idler lever depending on the mechanism mode.

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