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μPD72891,72893

IEEE1394 Link Layer Controller with DV Codec

Description

The μPD72891 and 72893 are a IEEE1394 link layer controllers developed for digital AV systems and feature an on-chip 32-bit RISC CPU (V850E) for IEEE1394 processing.

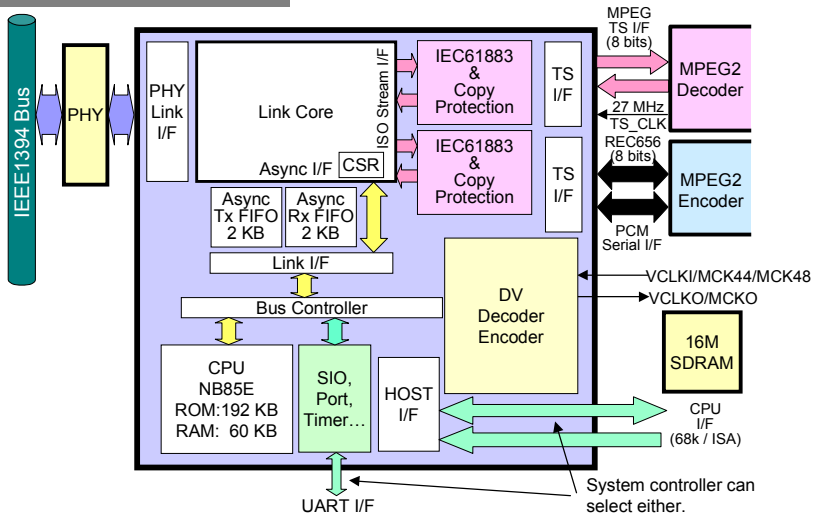
These link layer controllers have two stream interface channels to transmit/receive image data conforming to the IEC61883 Standard, such as MPEG and DV, and these channels can be independently used for transmission and reception. In addition, a total of 8 Kbytes of FIFO buffer space is provided to transmit/receive isochronous signals. This buffer space can be allocated as transmit and receive FIFO buffers in 2 Kbytes units.

The μPD72891 and 72893 support IEEE1394 bus control and AV/C commands via the on-chip CPU, as well as external control using either a serial or a parallel interface.

Features

- All functions required for Digital AV 1394 interface are equipped in a single-chip
  - On chip 32-bit RISC CPU
  - Copy Protection circuit equipped (the μPD72891 only)
  - Full duplex MPEG/DV transmission supported
  - On-chip IEC61883 function
- Compliant to IEEE1394-1995 and IEEE1394a-2000
- Supports 400 Mbps, 200 Mbps, 100 Mbps speed
- 3.3 V/2.5 V power supply
- Package : 208-pin QFP

Block Diagram of the μPD72891



Application and Companion Chip

- Application
  - Set-top Box
  - Digital VHS, DVD-RW, AV HDD
  - Digital Television
- Companion Chip
  - μPD72852 : 2-port low power PHY compliant with IEEE1394a-2000

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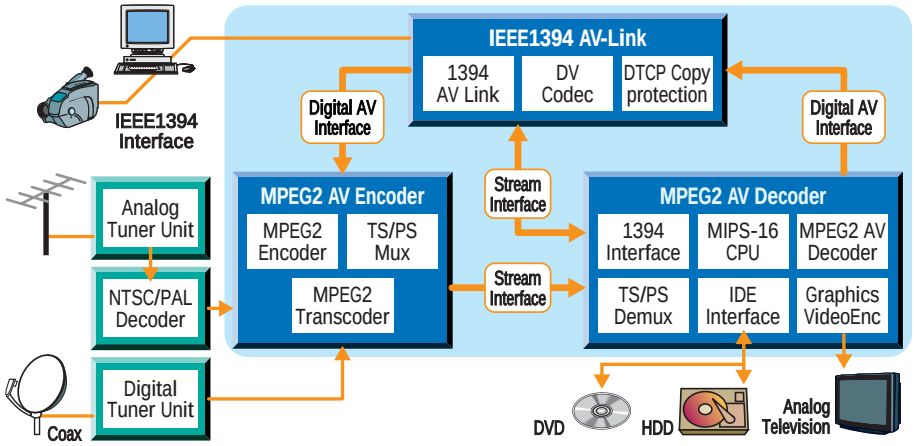
Device Solution for Digital AV



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