

IEEE1394 Link Layer Controller with DV Codec

The μ PD72891 and 72893 support IEEE1394 bus control and AV/C commands via the on-chip CPU, as well as external control using either a serial or a parallel interface.

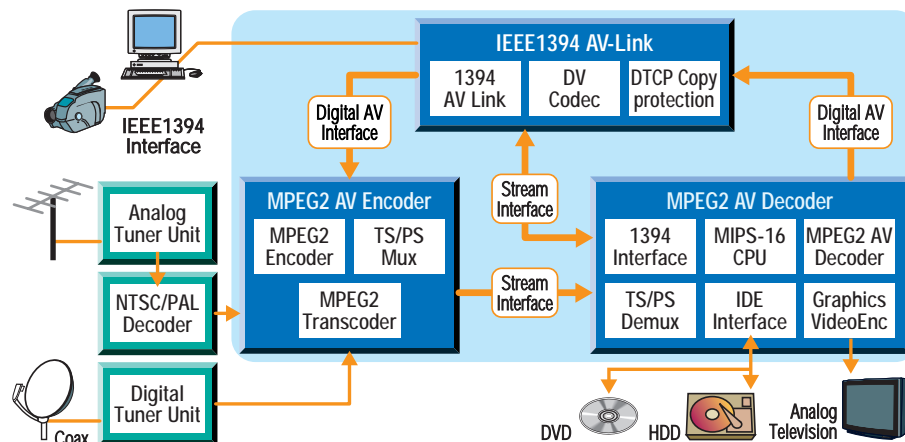
- All functions required for Digital AV 1394 interface are equipped in a single-chip
 - On chip 32-bit RISC CPU
 - Copy Protection circuit equipped (the μ PD72891 only)
 - Full duplex MPEG/DV transmission supported
 - On-chip IEC61883 function
- Compliant to IEEE1394-1995 and IEEE1394a-2000
- Supports 400 Mbps, 200 Mbps, 100 Mbps speed
- 3.3 V/2.5 V power supply
- Package : 208-pin QFP

The diagram illustrates the VLSI architecture for an MPEG2 decoder/encoder system. The system is connected to an IEEE1394 Bus via a PHY and a Link Core. The Link Core includes an Async I/F, CSR, and ISO Stream I/F. It interfaces with an IEC61883 & Copy Protection block, which is connected to a TS I/F. The TS I/F is connected to an MPEG2 Decoder and an MPEG2 Encoder. The MPEG2 Decoder outputs 27 MHz TS_CLK and REC656 (8 bits) to the MPEG2 Encoder. The MPEG2 Encoder outputs PCM Serial I/F to the DV Decoder Encoder. The DV Decoder Encoder outputs VCLKI/MCK44/MCK48 and VCLKO/MCKO to a 16M SDRAM. The 16M SDRAM is connected to the CPU I/F (68k / ISA). The CPU I/F is connected to the CPU (NB85E, ROM:192 KB, RAM: 60 KB). The CPU is connected to the SIO, Port, Timer... block, which is connected to the HOST I/F. The HOST I/F is connected to the UART I/F. The system controller can select either the CPU I/F or the UART I/F.

- Application
 - Set-top Box
 - Digital VHS, DVD-RW, AV HDD
 - Digital Television
- Companion Chip
 - μ PD72852 : 2-port low power PHY compliant with IEEE1394a-2000

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Device Solution for Digital AV



URL

<http://www.ic.nec.co.jp/>

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